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Quarterly Technical Report

Solid State Research

2003:3

Lincoln Laboratory

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

LEXINGTON, MASSACHUSETTS

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Massachusetts Institute of Technology
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Solid State Research

Quarterly Technical Report
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ABSTRACT

This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May through 31 July 2003. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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INTRODUCTION

1. QUANTUM ELECTRONICS

An external cavity tuning range of $\Delta\lambda = 0.3\ \mu m$, at a center wavelength $\lambda \sim 3.8\ \mu m$, has been demonstrated from an optically pumped, aluminum-free semiconductor laser grown on a GaSb substrate. The peak single-facet output power was 0.65 W, and an output power of >0.4 W was achieved over a tuning range of 180 nm.

2. ELECTRO-OPTICAL MATERIALS AND DEVICES

A model of tunneling resistivity between bonded semiconductor wafers has been developed. Narrow air gaps in the nanometer and subnanometer range between such wafers can give rise to considerable electron tunneling, and this tunneling can be further enhanced by a substantial potential barrier lowering that can be modeled by induced charges and image forces.

3. SUBMICROMETER TECHNOLOGY

Silicon micromachining techniques have been developed to fabricate knife-edge structures that taper to form 25-nm-wide tips. Pairs of these structures, placed knife edge to knife edge, form simple nanometer-scale probes that can be used to test molecular electronic devices.

A simulation package has been developed for predicting the impact of immersion, i.e., the presence of a uniform liquid layer between the last objective lens and the photoresist, on optical projection lithography. The improvement of process window afforded by immersion has been studied for a variety of conditions including $\lambda = 193$ and 157 nm, annular illumination, and the use of alternating phase shift mask technology.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

Two possible strataegies have been tested for the detection of toxin antigens using the CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) assay. The evidence to indicate the potential sensistivity of CANARY to toxins is discussed.

5. ADVANCED IMAGING TECHNOLOGY

Chemisorption charging, a method for treating the back surface of a back-illuminated *n*-channel image sensor, has been applied to charge-coupled devices and evaluated for low-energy x-ray spectroscopy. A thin film of Ag is used to form O^- ions in the thin SiO_2 layer grown on the sensor surface, which in turn aid in photoelectron charge collection; measurements of oxygen and carbon x rays show better energy resolution with this process than that of any of three other techniques we have used in recent years.

6. ANALOG DEVICE TECHNOLOGY

Initial circuit designs have been developed for the core elements of a Type-II quantum computer. The designs take into account several factors important in a quantum environment.

7. ADVANCED SILICON TECHNOLOGY

Total dose radiation effects from an x-ray source have been studied in submicron fully depleted *n*-channel field-effect transistors on conventional silicon-on-insulator wafers. A significant enhancement in radiation tolerance is observed both after substrate removal and after subsequent buried-oxide thinning.

REPORTS ON SOLID STATE RESEARCH
1 MAY THROUGH 31 JULY 2003

PUBLICATIONS

Accurate Analysis of the Magneto-Optical Permittivity Tensor of $Y_3Fe_5O_{12}$	G. A. Allen* G. F. Dionne	*J. Appl. Phys.* **93**, 6951 (2003)
Wavelength Beam Combining of Ytterbium Fiber Lasers	S. J. Augst A. K. Goyal R. L. Aggarwal T. Y. Fan A. Sanchez	*Opt. Lett.* **28**, 331 (2003)
Simulation Study of Process Latitude for Liquid Immersion Lithography	S.-Y. Baek* D. C. Cole* M. Rothschild M. Switkes M. S. Yeung* E. Barouch*	*Proc. SPIE* **5040**, Pt. 3, 1620 (2003)
Angle Resolved Scattering Measurements of Polished Surfaces and Optical Coatings at 157 nm	T. M. Bloomstein D. E. Hardy L. Gomez* M. Rothschild	*Proc. SPIE* **5040**, Pt. 2, 742 (2003)
Contamination Rates of Optical Surfaces at 157 nm: Impurities Outgassed from Construction Materials and from Photoresists	T. M. Bloomstein J. H. C. Sedlacek S. T. Palmacci D. E. Hardy V. Liberman M. Rothschild	*Proc. SPIE* **5040**, Pt. 1, 650 (2003)
Quantum Efficiency of PAG Decomposition in Different Polymer Matrices at Advanced Lithographic Wavelengths	T. H. Fedynyshyn R. F. Sinta W. A. Mowers A. Cabral	*Proc. SPIE* **5039**, Pt. 1, 310 (2003)

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Limits of Strong Shift Patterning for Device Research	M. Fritze R. Mallen B. D. Wheeler D.-R. W. Yost J. P. Snyder* B. Kasprowicz* B. Eynon* H. Y. Liu*	*Proc. SPIE* **5040**, Pt. 1, 327 (2003)
High-Power Nearly Diffraction-Limited AlGaAs-InGaAs Semiconductor Slab-Coubled Optical Waveguide Laser	R. K. Huang J. P. Donnelly L. J. Missaggia C. T. Harris J. J. Plant D. E. Mull W. D. Goodhue	*IEEE Photon. Technol. Lett.* **15**, 900 (2003)
Comparison of Detection Selectivity in Ion Mobile Spectrometry: Proton-Attachment Versus Electron Exchange Ionization	R. R. Kunz W. F. Dinatale P. Becotte-Haigh*	*Int. J. Mass Spectrom.* **226**, 379 (2003)
Accelerated Damage to Blank and Antireflectance-Coated CaF_2 Surfaces under 157-nm Laser Irradiation	V. Liberman M. Rothschild S. T. Palmacci N. N. Efremow J. H. C. Sedlacek A. Grenville	*Proc. SPIE* **5040**, Pt. 3, 1631 (2003)
Ambient Effects on the Laser Durability of 157-nm Optical Coatings	V. Liberman M. Rothschild S. T. Palmacci N. Efremow J. H. C. Sedlacek A. Grenville	*Proc. SPIE* **5040**, Pt. 1, 487 (2003)

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Improved Critical-Current-Density Uniformity by Using Anodization	D. Nakada K. K. Berggren E. M. Macedo V. Liberman T. P. Orlando*	*IEEE Trans. Appl. Supercond.* **13**, 111 (2003)
Intermodulation Distortion and Third-Harmonic Generation in YBCO Films of Varying Oxygen Content	D. E. Oates S.-H. Park M. A. Hein* P. J. Hirst* R. G. Humphreys*	*IEEE Trans. Appl. Supercond.* **13**, 311 (2003)
Ga Vacancies as Dominant Intrinsic Acceptors in GaN Grown by Hydride Vapor Epitaxy	J. Oila* J. Kivioja* V. Ranki* K. Saarinen* D. C. Look* R. J. Molnar S. S. Park* S. K. Lee* J. Y. Han*	*Appl. Phys. Lett.* **82**, 3433 (2003)
A B Cell-Based Sensor for Rapid Identification of Pathogens	T. H. Rider M. S. Petrovick F. E. Nargi J. D. Harper E. D. Schwoebel R. H. Mathews D. J. Blanchard L. T. Bortolin A. M. Young J. Chen* M. A. Hollis	*Science* **301**, 213 (2003)

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Fluorine: An Enabler in Advanced Photolithography	M. C. Rothschild T. M. Bloomstein T. H. Fedynyshyn V. Liberman W. A. Mowers R. Sinta M. Switkes A. Grenville K. Orvek	*J. Fluorine Chem.* **122**, 3 (2003)
Impact of Time-Ordered Measurements of the Two States in a Niobium Superconducting Qubit Structure	K. Segall* D. Crankshaw* D. Nakada T. P. Orlando* L. S. Levitov* S. Lloyd* N. Markovic* S. O. Valenzuela* M. Tinkham* K. K. Berggren	*Phys. Rev. B* **67**, 220506-1 (2003)
Experimental Characterization of the Two Current States in a Nb Persistent-Current Qubit	K. Segall* D. S. Crankshaw* D. Nakada B. Singh* J. Lee* T. P. Orlando* K. K. Berggren N. Markovic* S. O. Valenzuela* M. Tinkham*	*IEEE Trans. Appl. Supercond.* **13**, 1009 (2003)

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Improvement of *n*-GaN Schottky Diode Rectifying Characteristics Using KOH Etching	J. Spradlin* S. Dogan* M. Mikkelson* D. Huang* L. He* D. Jonstone* H. Morkoç* R. J. Molnar	*Appl. Phys. Lett.* **82**, 3556 (2003)
Immersion Liquids for Lithography in the Deep Ultraviolet	M. Switkes R. R. Kunz R. F. Sinta M. Rothschild M. Gallagher-Wetmore* V. J. Krukonis* K. Williams*	*Proc. SPIE* **5040**, Pt. 2, 690 (2003)
Large Splitting of the Cyclotron-Resonance Line in Al(x)Ga(1–x)N/GaN Heterostructures	S. Syed* M. J. Manfra* Y. J. Wang* H. L. Stormer* R. J. Molnar	*Phys. Rev. B* **67**, 241304-1 (2003)
Preliminary Microfluidic Simulation for Immersion Lithography	A. Wei* G. Nellis* A. Abdo* R. Engelstad* C.-F. Chen* M. Switkes M. Rothschild	*Proc. SPIE* **5040**, Pt. 2, 713 (2003)
Miniature, High-Power 355-nm Laser System	J. J. Zayhowski A. L. Wilson	*Proc. Trends Opt. Photon. Ser.* **83**, 357 (2003)

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PRESENTATIONS†

Wavelength and Coherently Combined Fiber Laser Arrays	T. Y. Fan	Technical Cooperation Program, MIT Lincoln Laboratory, Lexington, Massachusetts, 2 May 2003
AlGaAs/InGaAs 980-nm Slab-Coupled Semiconductor Lasers with Single-Spatial Large-Diameter Mode	R. K. Huang J. P. Donnelly J. N. Walpole* L. J. Missaggia C. T. Harris	Technical Cooperation Program, MIT Lincoln Laboratory, Lexington, Massachusetts, 2 May 2003
Aerosol Triggers	T. H. Jeys	Technical Cooperation Program, MIT Lincoln Laboratory, Lexington, Massachusetts, 2 May 2003
Passively *Q*-Switched Microchip Lasers and Applications	J. Zayhowski	Technical Cooperation Program, MIT Lincoln Laboratory, Lexington, Massachusetts, 2 May 2003
Fabrication Development for Superconducting Quantum Computing	K. Berggren W. Oliver J. Sage	Defense University Research Initiative on NanoTechnology (DURINT) Review, Stony Brook Manhattan, New York, New York, 5-6 May 2003

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† Titles of presentations are listed for information only. No copies are available for distribution.

Superconductive Approach to Type-II Quantum Computing	W. Oliver K. Berggren J. Sage	Defense University Research Initiative on NanoTechnology (DURINT) Review, Stony Brook Manhattan, New York, New York, 5-6 May 2003
Resist Materials for Advanced Lithography	T. H. Fedynyshyn	DARPA Program Review, Santa Fe, New Mexico, 5-8 May 2003
Liquid Immersion Optical Lithography	M. Rothschild M. Switkes R. R. Kunz R. Sinta T. M. Bloomstein	DARPA Program Review, Santa Fe, New Mexico, 5-8 May 2003
Interference and Noise Excision Techniques Based on High-T_c Superconductive Technology	L. M. Johnson	Dedicated Short Range Communications (DSRC) Workshop, Arlington, Virginia, 6 May 2003
Semiconductor Lasers for Infrared Countermeasures	A. Sanchez	Electro-Optical/Infrared Conference, Adelphi, Maryland, 15 May 2003
Photonic Components for RF Filtering and Wide-Band Antenna Nulling	M. Geis S. Spector R. Williamson T. Lyszczarz	Integrated Photonics Research/ Optics in Computing Topical Meeting, Washington, D.C., 16 May 2003
Coherent Beam Combining of Two 10-W Ytterbium Fiber Laser Amplifiers	S. J. Augst T. Y. Fan A. Sanchez	Solid State Diode Laser Technology Review, Albuquerque, New Mexico, 20-22 May 2003

975-nm and 915-nm AlGaAs-InGaAs Slab-Coupled Optical Waveguide Lasers	R. K. Huang J. P. Donnelly L. J. Missaggia C. T. Harris J. Plant W. D. Goodhue	Solid State Diode Laser Technology Review, Albuquerque, New Mexico, 20-22 May 2003
Fabrication of 3D Mode Converters for Silicon-Based Integrated Optics	M. Fritze J. Knecht C. Bozler C. Keast	47th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication, Tampa, Florida, 27-30 May 2003
A Method for Testing Electronic Self-Assembled Monolayers (SAMs) Using a Flip Chip Arrangement	S. J. Spector C. M. Wynn M. Switkes M. W. Geis R. R. Kunz S. J. Denneault M. Rothschild	47th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication, Tampa, Florida, 27-30 May 2003
Immersion Lithography: Extending Optics to 50 nm and Beyond	M. Switkes M. Rothschild R. R. Kunz R. Sinta S.-Y. Baek* D. C. Cole* M. Yeung* E. Barouch*	47th International Conference on Electron, Ion, and Photon Beam Technology and Nanofabrication, Tampa, Florida, 27-30 May 2003
MIT Lincoln Laboratory's Low-Power, High-Performance, Fully Depleted SOI CMOS Process Technology	C. L. Keast	NASA VLSI Design Symposium, Coeur d'Alene, Idaho, 28-29 May 2003

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CANARY B-Cell Sensor for Rapid, Sensitive Identification of Pathogens	J. D. Harper	3rd Annual Biodetection Technologies International Symposium, Arlington, Virginia, 1-3 June 2003
Development of Recovery Techniques for Organisms and Nucleic Acids from Complex Samples	L. Parameswaran L. Bortolin J. Harper M. Hollis C. Cabrera J. Bobrow B. Johnson	3rd Annual Biodetection Technologies International Symposium, Arlington, Virginia, 1-3 June 2003
Coherent Beam Combining of Ytterbium Fiber Laser Amplifiers	S. J. Augst T. Y. Fan A. Sanchez	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Three-Dimensional Imaging with Arrays of Geiger-Mode Avalanche Photodiodes	B. F. Aull A. Loomis D. Young A. Stern	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Laser-Induced Breakdown Spectroscopy for the Detection and Classification of Biological Aerosals	J. Hybl	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Active Optical Detection of Biological Agent Aerosols	T. H. Jeys	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003

Aerosol Triggers	T. H. Jeys	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Research at Lincoln Laboratory Leading to the Development of the Diode Laser	R. H. Rediker	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Short-Pulsed Nd:YAG/Cr^{4+}:YAG Passively *Q*-Switched Microchip Lasers	J. J. Zayhowski A. L. Wilson, Jr.	Conference on Lasers and Electro-Optics/Quantum Electronics and Laser Science Conferences, Baltimore, Maryland, 1-6 June 2003
Power Handling and Linearity of MEM Capacitive Series Switches	J. Muldavin C. Bozler C. Keast S. Rabe R. Boisvert	IEEE International Microwave Symposium, Philadelphia, Pennsylvania, 8 June 2003
Coherent Beam Combining and Noise Measurement of 10-W Ytterbium Fiber Laser Amplifiers	S. J. Augst T. Y. Fan A. Sanchez	Coherent Laser Radar Conference, Bar Harbor, Maine, 15-21 June 2003
Optical Lithography and the End of the Semiconductor Roadmap	M. Rothschild	Meeting of SPIE, New England Chapter, Newton, Massachusetts, 16 June 2003

MIT Lincoln Laboratory Capacitive Switch: Reliable RF MEMS for Antennas	J. B. Muldavin C. O. Bozler C. L. Keast M. A. Gouker J. Vian S. Targonski	IEEE Antennas and Propagation Society International Symposium, Ohio State University, Columbus, Ohio, 22-27 June 2003
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Non-contact Determination of Free Carrier Concentration in *n*-GaSb and *n*-GaInAsSb	C. A. Wang D. A. Shiau J. E. Maslar* W. S. Hurst*	Electronic Materials Conference, Salt Lake City, Utah, 25-27 June 2003
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1. QUANTUM ELECTRONICS

1.1 WIDELY TUNABLE, ALUMINUM-FREE GaSb-BASED, MID-INFRARED SEMICONDUCTOR LASERS

Wide wavelength tunability from mid-infrared laser sources operating in the $\lambda = 3–5$ μm range is of interest for both commercial and military applications. For chemical sensing applications, tunable and narrow linewidth sources are needed. For applications where high-power sources with good beam quality are needed, but where narrow spectral emission is not required, wavelength beam combining (WBC) is an attractive technique to scale spatial brightness [1],[2]. This is accomplished by wavelength multiplexing the emission from an array of lasers—each operating at a different wavelength—at a dispersive element such as a diffraction grating. For WBC, wide wavelength tunability is advantageous for combining larger numbers of laser elements.

Previously, external-cavity tuning in the mid infrared has been achieved using both quantum cascade lasers and optically pumped semiconductor lasers (OPSLs). External-cavity tuning of InP-based quantum cascade lasers has been reported with a tuning range of 0.14 μm and ~0.01 W of output power [3],[4]. External-cavity tuning of OPSLs, based on both GaSb/InAsSb double-heterostructure (DH) and InAs/InAsSb superlattices, has also been reported [5]. These OPSLs demonstrated peak output powers of ~0.1 and ~0.05 W, respectively, and tuning ranges of ~0.2 and ~0.3 μm, respectively. The ~0.3-μm tunability was achieved only by antireflection (AR) coating both front and back laser facets and by using short gain lengths ($L_c = 0.5$ mm) to suppress lasing of the isolated chip.

Over the past few years, significant advances have been made in GaSb-based, mid-infrared lasers that incorporate type-II "W" quantum wells (QWs) [6]. In particular, OPSLs based on the integrated absorber design possess many advantages for high-power applications [7]. In these lasers, the pump radiation is absorbed in GaInAsSb absorber layers, and the generated electron-hole pairs are transported to, and captured by, the QWs to provide optical gain. Recently, a further advancement of integrated absorber lasers was made in our laboratory by designing and demonstrating a laser structure that is free of aluminum-containing compounds [8]. Using lasers based on this design, researchers at the Air Force Research Laboratory have demonstrated >5 W of single-facet output power from a 2.5-mm-long device operating near 4 μm at 80 K [9].

A significant advantage of the aluminum-free laser designs in regard to external-cavity wavelength tunability is their reduced far-field beam divergence in the dimension normal to the plane of the epitaxial layers (fast axis). Previously, most GaSb-based OPSLs exhibited fast-axis far-field divergences in the range of 70–90° full width at half-maximum (FWHM). With aluminum-free lasers, in which the refractive index step between the GaInAsSb waveguiding core and the GaSb cladding is ~10× smaller than in previous designs, the beam divergence has been reduced to ~30° FWHM. This improves the wavelength tunability of external-cavity-controlled lasers because the threshold for lasing of the isolated chip can be significantly increased owing to (1) the ability to deposit lower-reflectivity AR facet coatings and (2) the reduced

single-pass modal gain resulting from the larger optical mode size. Furthermore, the coupling efficiency into the laser mode from the external cavity is improved because of increased power collection efficiency and reduced aberrations from the cavity optics.

Here, we demonstrate that sufficiently low reflectivity AR coatings are possible when using the aluminum-free design, such that lasing of the isolated chip was suppressed even at the highest available pump power. This enables the use of 2-mm-long lasers with only a single facet AR coated to achieve >0.3-μm tunability about 3.8 μm with 0.65 W of peak single-facet power.

The laser structure was grown by solid-source molecular beam epitaxy on a (100) *n*-GaSb substrate. Ten equally spaced type-II "W" QWs, each consisting of InAs/InGaSb/InAs (21Å/24Å/21Å), were embedded within the 1-μm-thick $Ga_{0.85}In_{0.15}As_{0.08}Sb_{0.92}$ integrated absorber. A 4-μm-thick GaSb cap layer served as the top optical cladding while the GaSb substrate served as the lower cladding. No aluminum was used in the growth of this laser structure.

The laser sample was thinned to ~100 μm to facilitate cleaving, metallized on the epi-side, AR coated at the $\lambda \sim 1.8$ μm pump wavelength on the substrate side, cleaved to create 2-mm-long lasers, and mounted epi-side down using In solder. Lasers were cooled in a liquid-nitrogen dewar and optically pumped using a $\lambda = 1.8$ μm InGaAs/InP diode laser array with a pump stripe width of ~150 μm on the OPSL. The fast-axis far-field divergence from the OPSL was measured to be 30° FWHM. Figure 1-1 plots the pulsed (35 μs, 2.5% duty cycle) single-facet output power vs input pump power at a heatsink temperature of 78 K. The peak power emitted per facet was measured to be 1.35 W at a pump power of 24 W. The free-running laser wavelength was 3.87 μm with a spectral width of 0.04 μm FWHM. A two-layer AR coating consisting of Al_2O_3 and TiO_2 was then applied to the output facet while the rear facet remained uncoated. As can be seen in Figure 1-1, this suppressed lasing from the device up to the highest pump power available.

The device was then placed in an external cavity, which is schematically depicted in Figure 1-2. The emission in the fast axis is collimated using an $f = 15$ mm ZnSe asphere. The Al_2O_3 $\lambda/2$-plate orients the polarization perpendicular to the grating lines to increase the diffraction efficiency. A 300-g/mm grating disperses the 1st-order diffracted radiation normal to the plane of the epilayers with a diffraction efficiency of ~80%. The intracavity ZnSe $f \cong 60$ mm cylindrical lens brings the beam in the slow axis to a focus at the output coupler to compensate for astigmatism in the beam emitted from the laser chip. The output coupler was the uncoated surface of a Ge window ($R = 36\%$), the opposite side of which was AR coated over $\lambda =$ 3–5 μm. The laser wavelength was tuned by rotating the output coupler. The output power was measured after the output coupler while the 0-order diffracted beam from the grating was used to monitor the laser spectrum.

In Figure 1-3, the normalized spectra from the laser as it was tuned across 3.632–3.934 μm are overlapped on a linear scale. These spectra were taken within a time gate of ~3 μs. Note that the tuning is clean with no indication of parasitic lasing. Also plotted in Figure 1-3 is a high-resolution scan of the laser tuned to 3.877 μm. The measured linewidth of 0.6 nm FWHM is limited by the spectrometer resolution. The side-mode suppression ratio (SMSR) is 27 dB with respect to, in this case, a secondary laser mode

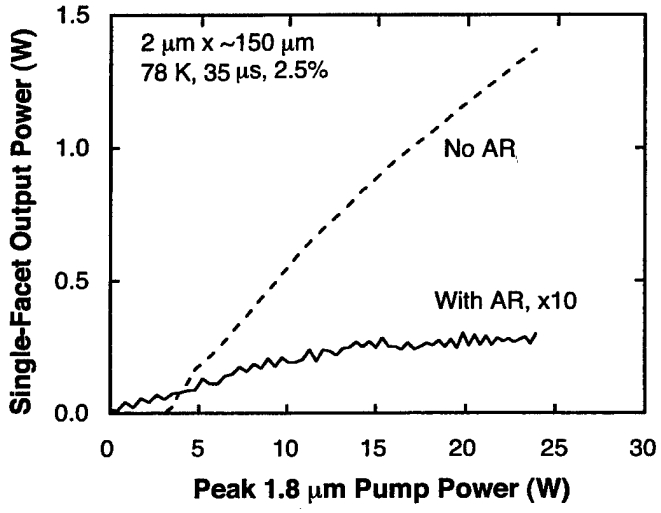

Figure 1-1. Single-facet output power as a function of incident pump power both with and without a front-facet antireflection coating.

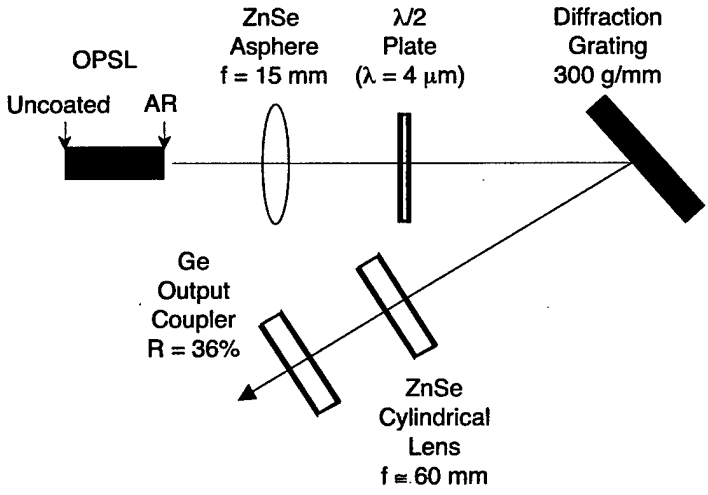

Figure 1-2. External cavity configuration.

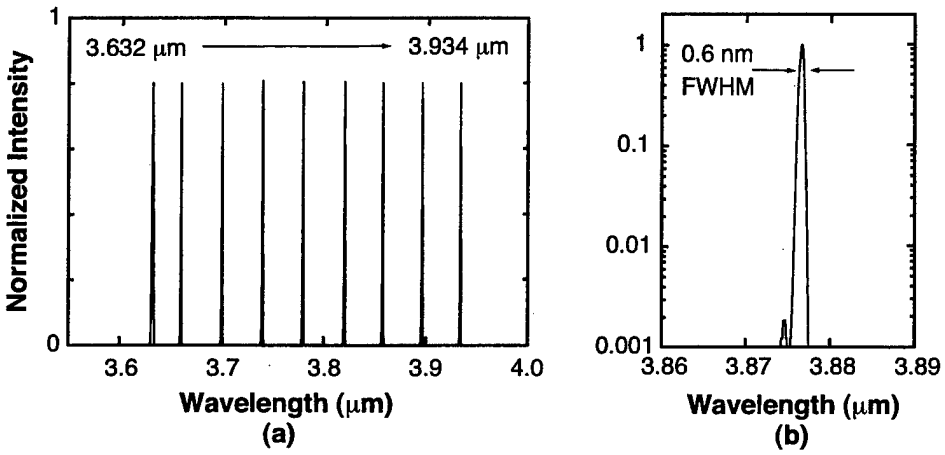

Figure 1-3. (a) Normalized spectra of laser as it is tuned in wavelength and (b) high-resolution scan of a single laser line at a pump power of 24 W and T = 78 K.

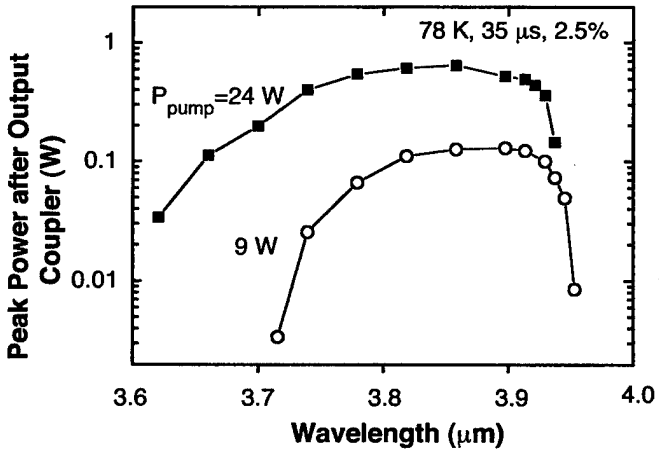

Figure 1-4. Output power as a function of lasing wavelength for two pump powers.

offset by ~2 nm from the main laser peak. It is unclear what gives rise to the secondary peak since the chip modes are spaced by ~1 nm. Based on the cavity and grating geometry, the instantaneous linewidth should be <0.2 nm. In any case, the laser is most probably operating on multiple longitudinal modes of the external cavity since these are spaced by only 0.001 nm. Even to the edges of the tuning range, SMSR was found to be greater than ~20 dB, and the laser linewidth remained below the spectrometer resolution.

Figure 1-4 plots the power after the output coupler as a function of lasing wavelength for two different pump powers. At a pump power of 9 W, the peak power is ~0.1 W and the tuning range extends from 3.71 to 3.95 μm. At a pump power of 24 W, the peak power increases to 0.65 W at $\lambda = 3.85$ μm and the tuning range extends from 3.62 to 3.94 μm. The tuning range over which the output power is >0.4 W is 180 nm. Since the isolated laser chip did not lase, modulation of the output power with wavelength tuning was only discernable at the extreme edges of the tuning range. With regard to WBC, this bandwidth is sufficient to combine beams from a ~1-cm-wide laser bar with external cavity dimensions of only a few 10's of centimeters.

Finally, it should be noted that by reducing the intracavity loss and optimizing the output coupler reflectivity, we anticipate that the output power can be comparable to that of the uncoated, free-running laser. Furthermore, by applying a high-reflectivity coating to the back facet, a substantial power increase can be expected.

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2. ELECTRO-OPTICAL MATERIALS AND DEVICES

2.1 MODEL OF TUNNELING RESISTIVITY BETWEEN BONDED SEMICONDUCTOR WAFERS

Electrical conduction across the bonded interface is a basic issue in semiconductor wafer bonding. Recent measurement of a 1.3-nm average air gap between GaP wafers bonded by van der Waals force [1] points to a possibility for considerable electron tunneling. Here, we develop a model to estimate the tunneling current and the equivalent electrical resistance of the bonded interface.

For a free electron traveling in one dimension with energy E, the probability to tunnel through a square potential barrier of height V_0 ($>E$) and width a is well known [2]:

$$T_{\text{tunnel}} = \left[1 + \frac{\left(k^2 + \kappa^2\right)^2}{4k^2\kappa^2}\sinh^2 \kappa a\right]^{-1} \tag{2.1}$$

where

$$k \equiv \left(\frac{2mE}{\mathrm{h}^2}\right)^{1/2} \tag{2.2}$$

$$\kappa \equiv \left(\frac{2m\left(V_0 - E\right)}{\mathrm{h}^2}\right)^{1/2} \tag{2.3}$$

m is the electron mass, and h is the Planck constant. When $V_0 >> E$, the tunneling probability is generally small, depending exponentially on the barrier width a and the square root of the barrier height, $V_0^{1/2}$.

For bonded n-type Si wafers (without an oxide bonding layer), the potential barrier would be the electron affinity $\chi_e = 4.05$ eV, which is the energy needed to remove one electron from the material (from the bottom of the conduction band E_c) to infinity in vacuum. However, the potential builds up over a distance of a few angstroms, and can be modeled by an effective image force, i.e., the Schottky effect, in which the electron is attracted to the material by an induced surface charge [3]–[5]. This can result in considerable barrier lowering in high field [3],[4] or, as in the present case, in close proximity [5].

To model the barrier lowering, consider first the conventional image-force potential energy for an electron at a distance r from the surface of a semi-infinite dielectric medium [6]

$$V(r) = -\frac{\varepsilon - 1}{\varepsilon + 1}\frac{e^2}{4r} \tag{2.4}$$

where ε is the dielectric constant (ε = 12.0 for Si) and e is the elementary charge. However, Equation (2.4) cannot be applied to extremely small distances, and it diverges when $r \rightarrow 0$. A small modification can nonetheless be made:

$$V(r) = -\frac{\varepsilon - 1}{\varepsilon + 1}\frac{e^2}{4(a_0 + r)} \tag{2.5}$$

which produces the correct χ_e (i.e., $V(0)$ = –4.05 eV) with $a_0 \equiv 0.75$ Å. Equation (2.5) implies that the induced charge is effectively located at a small distance a_0 below surface. This is consistent with the picture that the induced charges are positive ions, whose centers are the effective location of the charges. It is also worth noting that a_0 of 0.75 Å is between the atomic and ionic (inert gas configuration) radii of Si, which are 1.17 and 0.41 Å, respectively [7].

Based on this model, the potential barrier between the Si surfaces separated by a gap distance a is given by

$$V(x) = \frac{\varepsilon - 1}{\varepsilon + 1}\frac{e^2}{4}\left[\frac{1}{a_0} - \frac{1}{\left(a_0 + \frac{a}{2} + x\right)} + \frac{1}{a_0 + a} - \frac{1}{\left(a_0 + \frac{a}{2} - x\right)}\right] \tag{2.6}$$

where the origin ($x = 0$) is now conveniently chosen at the mid point in the air gap. Note that Equation (2.6) reflects an image charge in each of the two wafers, but the higher-order images are neglected. Figure 2-1 shows an example of the potential barrier for a = 4 Å. Note that there is considerable barrier lowering in comparison to χ_e of 4.05 eV.

Since the solution of the Schrödinger equation with this potential barrier is not known, an effective square potential V_0 is used in this model, with V_0 given by

$$\left(\frac{2mV_0}{\mathrm{h}^2}\right)^{1/2} a = \int_{-a/2}^{a/2}\left(\frac{2mV(x)}{\mathrm{h}^2}\right)^{1/2} dx \tag{2.7}$$

This effective barrier height V_0 has been numerically evaluated as a function of the air gap thickness a, as shown in Figure 2-2. Note that except for very small a, below 0.5 Å, this effective barrier height is generally much greater than the thermal energy, and hence $V_0 >> E$. Equations (2.1) and (2.3) can then be simplified considerably, but such simplification is not used in the following numerical calculations.

To calculate the tunneling probability using Equation (2.1), the electron wave number k in the direction of the surface normal, i.e., the x direction, needs to be evaluated. Considering the Si energy band structure with ellipsoids of constant energy E in the **k** space, the average $\overline{k_x^2}$ is given by

$$\overline{k_x^2} = \frac{1}{3}\frac{2m^* E}{\mathrm{h}^2} \tag{2.8}$$

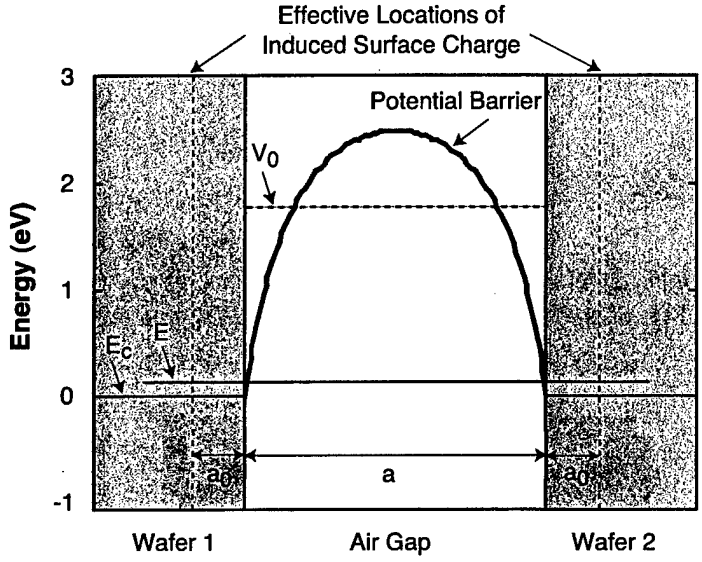

Figure 2-1. Modeled potential barrier for electron tunneling between two Si wafers separated by an air gap a of 4 Å, and the schematic diagram of physical parameters used in the calculation of the tunneling resistivity. Note that the barrier is significantly lower than the usual electron affinity of 4.05 eV.

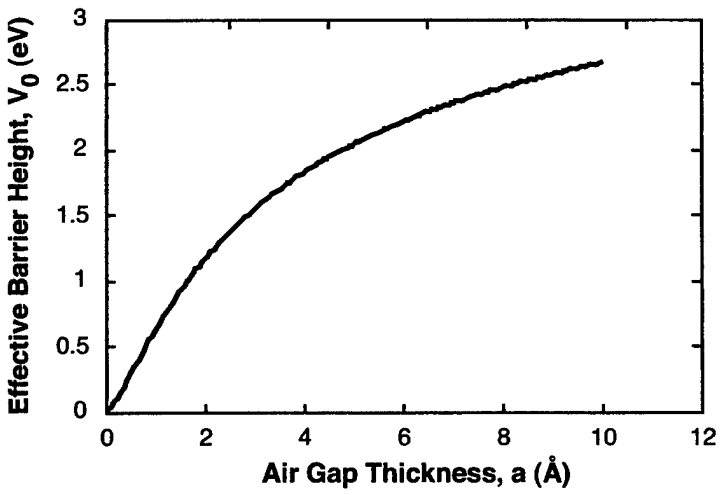

Figure 2-2. Modeled effective barrier height, V_0, as a function of the air gap thickness, a, between Si wafers.

where the electron effective mass is given by

$$\begin{aligned} m^* &= \frac{1}{3}\left(m_\ell^* + 2m_t^*\right) \\ &= \frac{1}{3}(0.98m + 2\times 0.19m) \\ &= 0.45m \end{aligned} \tag{2.9}$$

For moderate to high doping levels where the electron Fermi energy E_F is still below the bottom of the conduction band E_c, the Maxwell-Boltzmann statistics can be used, and the average electron energy $\langle E \rangle$ is given by

$$\langle E \rangle = \frac{3}{2} k_B T \tag{2.10}$$

where k_B is the Boltzmann constant, T is the absolute temperature, and $k_B T$ = 0.026 eV at room temperature. Equations (2.8)–(2.10) yield the average $\overline{k_x^2}$, which is then used in Equation (2.1) to calculate T_{tunnel}. Figure 2-3 shows the calculated tunneling probability as a function of the air gap thickness a. For comparison, the tunneling probability for $V_0 \equiv \chi_e$ (i.e., without barrier lowering) is also calculated and is generally nearly 2 orders of magnitude lower.

As can be seen in Figure 2-3, most tunneling occurs in the first few angstroms of the air gap thickness. Recent measurement on wafer-bonded GaP/GaP showed an average air gap thickness of 13 Å [1]. This indicates a close contact between wafers, limited probably by the atomic steps in the polished surfaces. Assuming that Si has a similar polished surface and the bonded wafers have a linearly graded gap thickness from 0 to 26 Å, the average tunneling probability $\overline{T_{tunnel}}$ is then 0.029.

When a small bias voltage ΔV is applied across the air gap, the Fermi level on one side is raised against the other side, and in the Maxwell-Boltzmann statistics the resulting excess electron concentration (capable of producing a net tunneling current) is given by

$$\begin{aligned} \Delta n &\cong n\left[\exp\left(\frac{e\Delta V}{k_B T}\right) - 1\right] \\ &\cong n\frac{e\Delta V}{k_B T} \end{aligned} \tag{2.11}$$

where n is the total electron concentration. Assuming low state occupation, i.e.,

$$\exp\left(-\frac{E - E_F}{k_B T}\right) << 1 \tag{2.12}$$

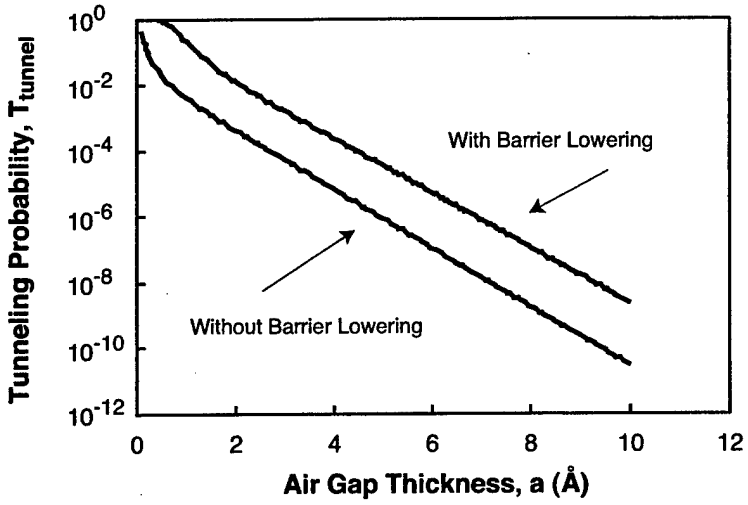

Figure 2-3. Tunneling probability as a function of air gap thickness, a, calculated by using the modeled barrier height, V_0.

the tunneling current density j is given by

$$j = \frac{1}{2} e \Delta n \overline{v_x T_{\text{tunnel}}} \tag{2.13}$$

where the numerical factor 1/2 reflects the probability of an electron moving toward, i.e., not away from, the air gap, and $\overline{v_x}$ is the average electron velocity in that direction. An averaging similar to that which led to Equation (2.8) puts $\overline{v_x}$ at 1.1×10^7 cm/s.

An equivalent series resistivity can now be defined and evaluated

$$\begin{aligned} \rho_{\text{tunnel}} &\equiv \frac{\Delta V}{j} \\ &= \frac{k_B T / e}{e n \overline{v_x T_{\text{tunnel}}}} \end{aligned} \tag{2.14}$$

where the last step is made by using Equations (2.11) and (2.13). Substituting the modeled $\overline{T_{\text{tunnel}}}$ of 0.029 and other given material parameters in Equation (2.14), we have for $n = 3 \times 10^{18}$ cm^{-3}

$$\rho_{\text{tunnel}} = 3.5 \times 10^{-7} \ \ \Omega \cdot \text{cm}^2 \tag{2.15}$$

This is relatively low compared to most contact resistivities and is favorable for applications. However, it should be noted that $\overline{T_{\text{tunnel}}}$ is sensitive to the thickness profile of the air gap, which is not specified by the previous experimental measurement of the averaged thickness.

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3. SUBMICROMETER TECHNOLOGY

3.1. METHOD FOR TESTING ELECTRONIC SELF-ASSEMBLED MONOLAYERS USING A FLIP-CHIP ARRANGEMENT

Molecular devices offer the possibility of fabricating nanometer-scale electronic circuits, and represent the ultimate scaling of electronic components. Consequently, the synthesis and testing of new molecular compounds is currently a very active research area. The electronic testing, in particular, has been a difficult problem because of the difficulty in probing at the molecular level. We describe a novel testing method based on flip-chip structures fabricated with standard micromachining techniques. Once the test structures have been fabricated, it is possible to perform measurements on any suitable molecules using only simple equipment.

The method for making measurements using the flip-chip structures is shown in Figure 3-1. Each chip contains a sharp knife edge, contact pads, and stand-offs. The knife edge is fabricated by an anisotropic wet etch of silicon creating a narrow peak with widths of about 30 nm. This knife edge and the contact pads are coated with gold for self-assembled monolayer (SAM) formation and electrical continuity. The stand-offs are fabricated with an electrical insulator on top and are 100 nm taller than the knife edge. Depending on the experiment, the SAM to be tested is grown on the gold of one or both chips. To perform the measurement, the two chips are placed together with the top chip flipped upside down and rotated 90° relative to the bottom chip. The height difference between the stand-offs and the knife edge creates a gap

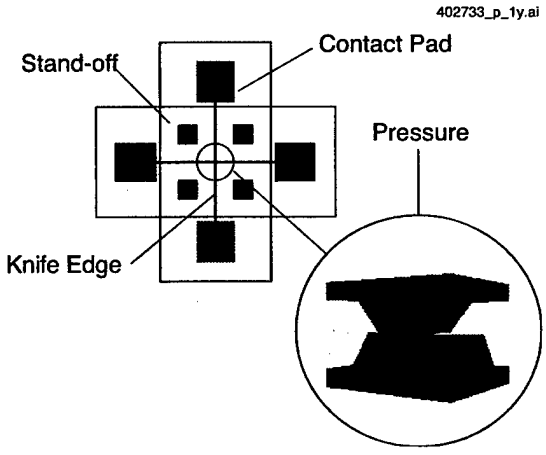

Figure 3-1. Two chips in flip-chip arrangement. Note that features that would be hidden by the top chip are shown. Each chip contains four stand-offs and two contact pads connected by a knife edge. The inset shows a cross-sectional view of the contact between the two chips. Because of the stand-offs, there is a small gap between the two knife edges. Pressure is applied to bring the knife edges into contact.

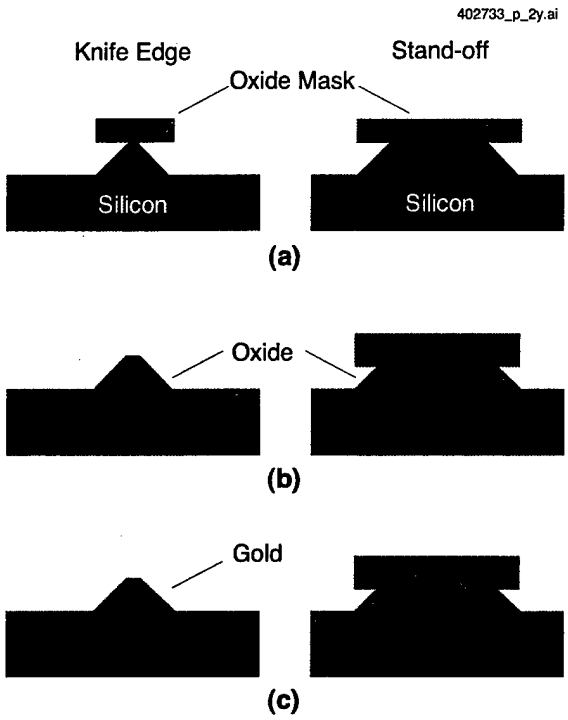

Figure 3-2. Fabrication process for flip-chip devices. The left column shows the fabrication of the knife edge, and the right column shows the simultaneous fabrication of the stand-offs. (a) An oxide mask is fabricated by a standard dry etch, and the silicon is etched by an anisotropic wet etch. (b) The oxide mask is stripped off the knife edge (and contact pads), and a 30-nm oxide is grown everywhere. (c) Gold is deposited on the knife edge (and contact pads) by a lift-off process.

between the knife edges of the two chips. Pressure is applied to the top chip, bending the silicon substrate and bringing the knife edges into contact in a controlled, reproducible manner that does not damage the SAM. Once contact is made, electrical measurements can be performed by passing current between the two chips, across the SAM.

The process used to fabricate the flip-chip devices is outlined in Figure 3-2. The steps are knife-edge and stand-off definition, silicon oxide growth for isolation, and gold lift-off to coat the knife edge and contact pads. The most challenging step is the creation of the knife edge. First, deep-UV optical lithography and plasma etching are used to pattern 130–230-nm-wide lines in a 120-nm-thick silicon dioxide hard mask. To form the triangular profile in the silicon, the sample is wet etched for about 100 s in tetramethyl ammonium hydroxide (TMAH) heated to 90°C. This etch is very selective for silicon over the oxide, and the size of the oxide mask is unchanged during the etch. The TMAH etch chemistry is also anisotropic [1],[2] and etches the (111) crystal plane very slowly, which creates a silicon profile with a 54.7° sidewall, and prevents the oxide mask from being undercut. Some undercutting does still occur,

likely due to imperfect alignment between the lithography of the oxide mask and the crystal planes of the silicon wafer. This process has produced 30-nm-wide peaks starting with a ~190-nm-wide mask feature. Because 190-nm features are routinely obtainable using optical lithography, this technique offers a practical method for creating 30-nm features using standard lithography tools.

After the TMAH etch, a low-resolution lithography step is used to protect the oxide on the stand-offs from the buffered oxide etch, which strips the oxide mask from the knife edge and the contact pads. This oxide causes the stand-offs to be taller than the knife edge, creating the desired gap between knife edges when two chips are used in the flip-chip arrangement.

The final two steps are silicon oxide growth and gold deposition. For isolation of the conducting gold features from the substrate of the chip, a 30-nm-thick oxide is grown by dry oxidation over the entire chip. Then, a gold lift-off is done to coat the knife edge and contact pads with gold. Because it is merely necessary to coat the knife edge, fairly low resolution lithography is sufficient for this step. (Arbitrarily, a 3-μm-wide line of gold is patterned on the knife edge.) Although gold is incompatible with CMOS processing, all steps up to the gold deposition, including the photolithography used to define the gold, can be done using a CMOS toolset. After the final photolithography step, 20 nm of gold is deposited on top of a 5-nm adhesion layer of titanium in a separate cleanroom. The knife edge of a finished device is shown in Figure 3-3. Some rounding of the peak occurs from the oxide growth and gold deposition. This rounding does not affect the contact area of the knife edge adversely, and, in fact, shrinks the effective contact area to ~25 nm. After gold lift-off the chips can be diced, and SAMs can be grown on the chips as desired.

Figure 3-4 shows a diagram of the apparatus used to make measurements with a pair of chips. Depending on the desired measurement, SAMs are first grown on one or both chips. As mentioned above, the two chips are put together facing each other, with one chip rotated 90°. The bottom chip is held firmly by a vacuum. The top chip lies somewhat freely on top of the bottom chip with its stand-offs resting on the bottom chip's stand-offs. Because the stand-offs are large (1.5 × 1.5 mm), it is easy to place the top chip. In addition, the top chip can be moved to contact multiple locations of both knife edges for multiple clean measurements on the same sample.

Initially, there is a gap of about 190 nm between the knife edges, corresponding to the height of the oxide minus the height of the gold of both chips. Force is applied to the top chip to flex it and bring the knife edges into contact. To precisely control the amount of force, a beaker of water is mounted on a piston that presses down on the chip, as shown in Figure 3-4. About 500 g of weight is necessary to make contact, indicating a deflection rate of 0.4 nm/ml. This agrees reasonably well with a value of 0.27 nm/ml calculated using a simplified model of a beam resting on two contact points [3]. Because water in amounts significantly less than 1 ml can be added or removed, the deflection can be controlled to less than an angstrom. To make contact, water is added at a rate between 1 and 5 ml/min while the current flowing between the chips is monitored to determine contact. When the current increases above a threshold, typically about 1 nA with a dc voltage of 1 V, contact has been detected and the addition of water stops. This process is automated, and making contact typically takes about 10 min. After contact is made, the electrical properties of the SAM can be probed by varying the voltage and measuring the current.

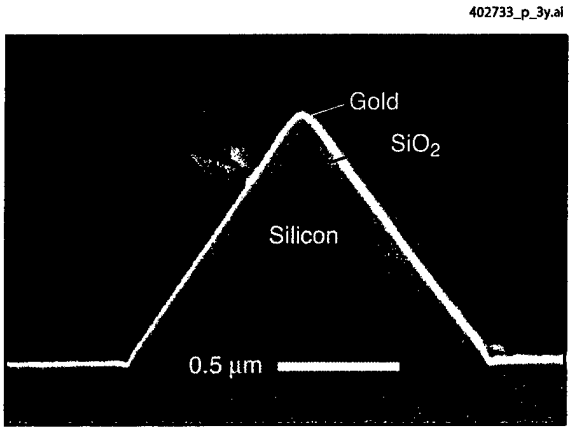

Figure 3-3. Cross-sectional scanning electron micrograph of a completed knife edge. The sample is positioned at an angle of 90°. (Some debris from the cleave is visible.)

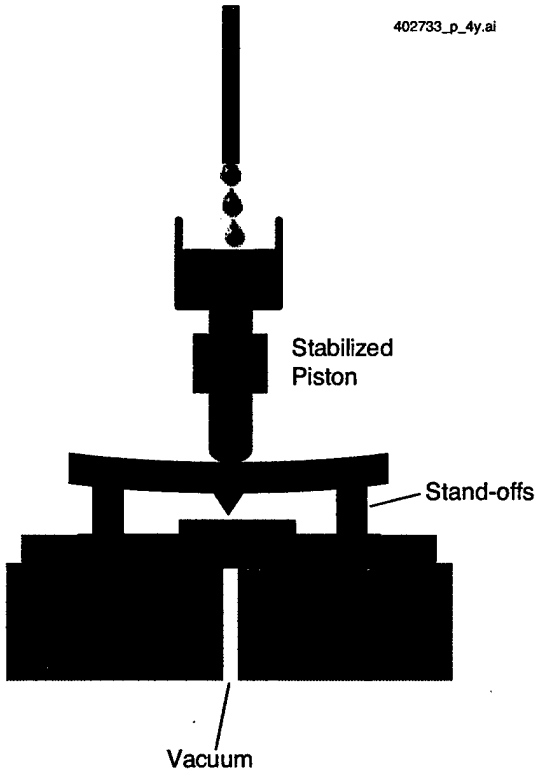

Figure 3-4. Diagram of apparatus used to make measurements.

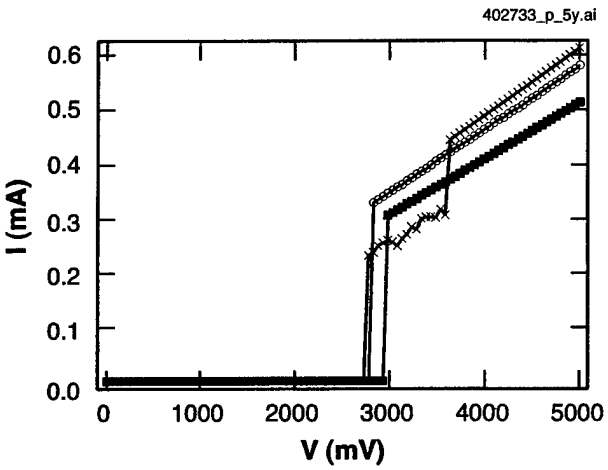

Figure 3-5. Breakdown measurements made on three alkanethiol samples of C-14 molecules. When the voltage reaches 2900 mV, breakdown occurs and the conductivity of the junction increases dramatically.

To demonstrate the method, electrical measurements were made on SAMs of an alkanethiol. Molecules of this type form highly resistive SAMs and have been studied by others [4],[5]. For this experiment, a SAM of an alkanethiol with a 14 carbon chain (C-14) was grown on the top chip. Prior to growing the SAM, the chip was cleaned in a piranha solution. To grow the SAM, the chip was submersed in a solution of alkanethiol dissolved in ethanol for 24 h. After contact was made using the above procedure, the breakdown voltage of the SAM was measured. This is done by increasing the voltage until breakdown occurs and the conductance of the junction greatly increases. Figure 3-5 is a current-voltage (I-V) plot showing three breakdown measurements. Breakdown occurs at 2.9 V with good repeatability. This value agrees with reported measurements [4] done by scanning probe microscopy on a 12-carbon-long alkanethiol, where the breakdown voltage was 2.5 V.

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3.2. SIMULATION STUDY OF PROCESS LATITUDE FOR LIQUID IMMERSION LITHOGRAPHY

Liquid immersion lithography is a promising candidate for the micro/nanolithography technology roadmap for critical dimensions (CDs) down to perhaps 45 nm. A simulation package, as described here, has been developed to address the critical optical issues associated with immersion technology. The package accounts for high numerical aperture (NA) imaging, via a full Maxwell vector solution approach,

including polarization effects, as well as accounting for multilayers of thin film media of arbitrary complex index of refraction. This simulation capability was used to examine the process window for line and space structures, based on depth of focus (DOF), for a wide range of conditions: 193- and 157-nm wavelength projection systems, NA ranging between 0.9 and 1.3, and circular and annular illumination schemes, as well as alternating phase shift mask (PSM) structures. Liquid immersion is predicted to significantly improve printability between 45- and 90-nm CD, with changes in NA required at specific CD junctions to remain on the optimal operating curve.

Our model of liquid immersion lithography is shown in Figure 3-6. The space between the final optical element of the projection lens, represented in Figure 3-6 by a hemispherical lens, and the resist-coated wafer is assumed to be filled with a high-index liquid. This permits exposure with incident light of large obliquity that would otherwise be totally internally reflected at the optic-air interface of a dry exposure system [6]. A light ray of wavelength λ in air entering the hemispherical lens of refractive index n_{lens} at an angle θ_{lens} contributes to an image spatial frequency $f = n_{lens}\sin\theta_{lens}/\lambda$. For a ray passing next to the rim of the lens pupil, this corresponds to NA = $n_{lens}\sin\theta_{lens} = n_{liquid}\sin\theta_{liquid}$, where n_{liquid} is the liquid refractive index (assumed to be real for the present discussion) and θ_{liquid} is the propagation angle of the ray in the liquid. In order for the ray to propagate through the liquid, the NA must satisfy NA < n_{lens} or n_{liquid}, whichever is less. The modeling software computes the aerial image for the liquid immersion optical system described above. Vector and thin-film interference effects are taken into account [7] to allow simulation of the image intensity distribution inside the resist layer. High-NA effects are also taken into account by the use of a suitable high-NA factor [8],[9].

We begin a discussion of our simulation results by examining predictions of the contrast in printability of a large array of equal lines and spaces. The software can calculate the light intensity throughout the entire thickness of the photoresist. However, since many resist chemistries are still under consideration for immersion lithography [10], and hence the resist parameters are not yet defined, we

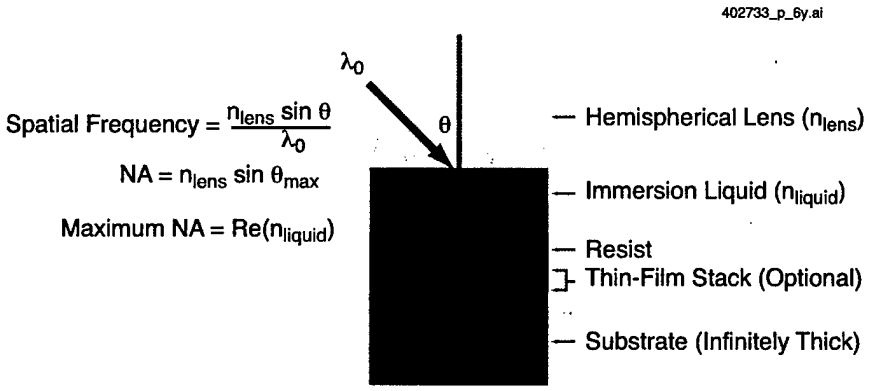

Figure 3-6. Physical picture of liquid immersion microlithography. The software that has been developed to simulate this arrangement can handle an arbitrary number of layers of films in the "thin-film stack," with each film described by a single complex index of refraction.

concentrate on the light intensity just below the surface of the resist, taking into account the influence of the liquid-resist interface but not the absorbance or other properties of the bulk of the resist itself. We use the conventional aerial image threshold model procedure [11],[12] to estimate the printability of such structures. Despite the simplicity of this model, the general *trends* should still hold even when more realistic resist properties are later taken into account.

The following results will be based on the light intensity calculated in the top part of the photoresist, which is taken to be sufficiently thick as to prevent reflection from the Si substrate. The various layers have the following indices: $\tilde{n} = 0.6644 + 2.04i$ for the underlying silicon, $\tilde{n} = 1.52 + 0.03i$ for the photoresist at λ = 193 nm, and $\tilde{n} = 1.4 + 0.03i$ for the photoresist at λ = 157 nm, and $\tilde{n} = 1.47$ (water) and $\tilde{n} = 1.38 + 10^{-5}i$ (perfluoropolyether) for the immersion liquids at λ = 193 nm and 157 nm, respectively. All results assume unpolarized incident light. The immersion liquid thickness is taken to be 1 mm at 193 nm and 0.1 mm for 157 nm. These values reflect our best estimates for the appropriate parameters given the current state of immersion lithography [10] at 193 and 157 nm; they will undoubtedly need to be refined as the technologies develop. Still, the general conclusions drawn from the present simulations should remain valid.

Our initial results use contrast calculations to estimate the printability of a given aerial image. Later, we turn to exposure-defocus calculations, following conventions often discussed in B. Lin's works [13]. The contrast

$$C = \frac{I_{\max} - I_{\min}}{I_{\max} + I_{\min}} \tag{3.1}$$

was calculated just below the surface of the photoresist. Figure 3-7 shows curves of contrast vs focus for four sets of equal lines and spaces with dimensions of 75, 65, 55, and 45 nm exposed with a binary mask under circular illumination with σ = 0.6. In each case, curves for NA = 1.1 and 1.3 at 193 nm and NA = 0.9 and 1.3 at 157 nm are shown. All exposures except the NA = 0.9 case are made in liquid immersion. If we take a contrast of 0.3 as an acceptable level of printability, then a reasonable estimate of the DOF can be calculated from these and other similar plots. In Figure 3-7(a), all four wavelength/NA combinations can print 75-nm line/space features, with the largest DOF occurring for the NA = 1.1, λ = 93 nm case. As expected, for a given wavelength, as NA increases, one can obtain a higher level of contrast when in best focus; however, DOF is typically negatively affected.

A better perspective is shown in Figures 3-8(a) and 3-8(b). At any given feature size, of course one wants the largest DOF in order to have as large a process window as possible. Hence, by "walking" along the upper envelope of each of the curves in Figures 3-8(a) and 3-8(b), we see roughly the desired point at each stage to best take advantage of liquid immersion capability.

Thus, liquid immersion technology offers the ability of increasing the maximum range of NA beyond unity, as well as providing a vehicle to select the most appropriate NA value for printing the features of interest, with the maximum DOF allowable. In addition, liquid immersion technology can be

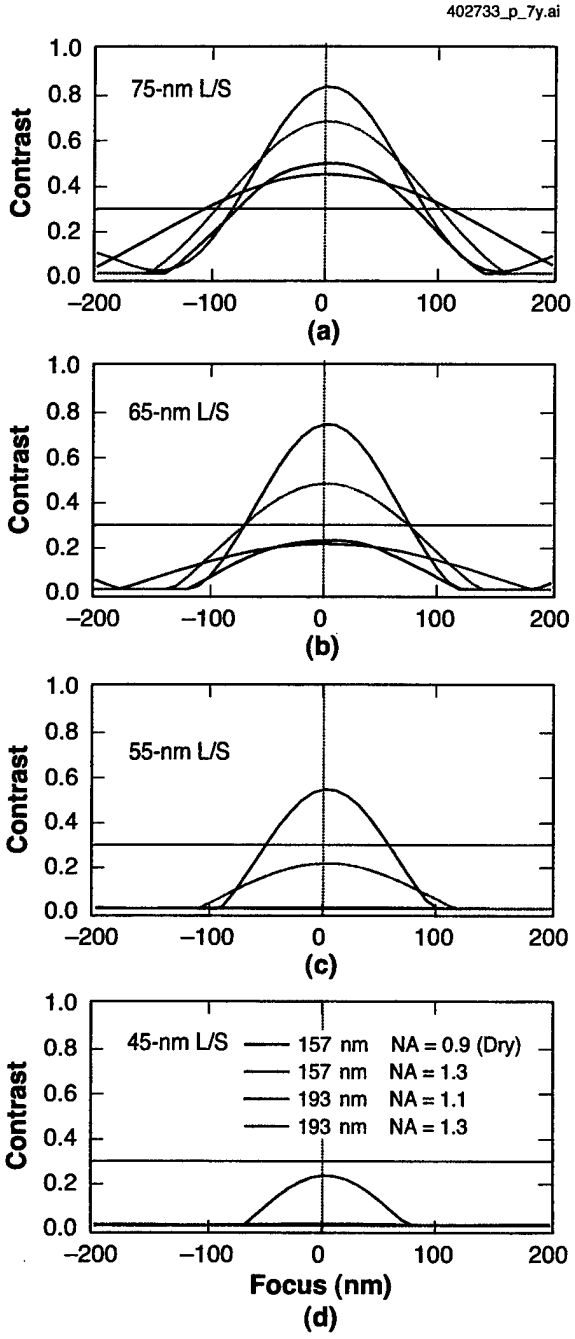

Figure 3-7. Contrast vs focus for 1:1 line/space (L/S) structures exposed with a binary mask and circular illumination (σ = 0.6).

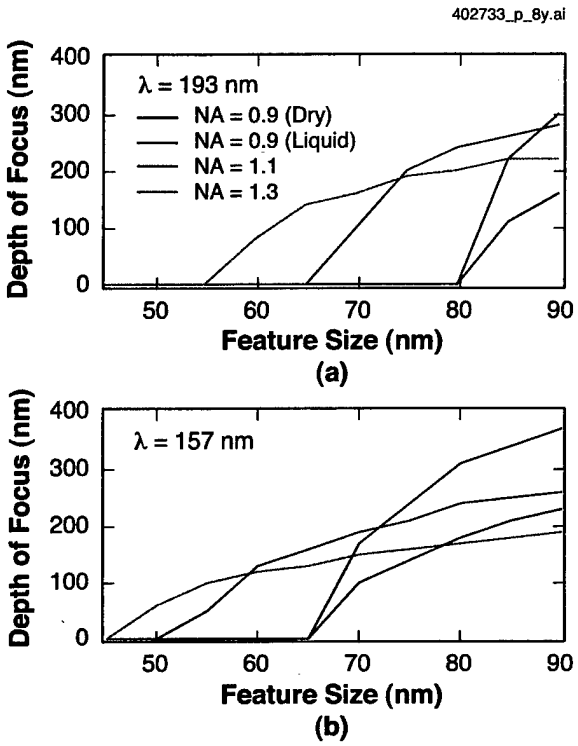

Figure 3-8. Depth of focus (DOF) vs feature size with a binary mask and circular illumination for (a) λ = 193 nm and (b) λ = 157 nm, as calculated from the information in Figure 3-7.

readily combined with other well-known resolution enhancement techniques [14], such as off-axis illumination, optical proximity correction, PSM techniques, and focus-latitude enhancement exposure methods [15], thereby pushing the limits suggested by Figure 3-8.

Figures 3-9(a) and 3-9(b) provide an indication of how annular illumination, characterized by inner and outer radial parameters of 0.4 and 0.6, respectively [9], complements immersion. In Figure 3-9(a), we see that this annular partial coherence condition improves the DOF for printing 65-nm lines and spaces at NA = 1.3, λ = 193 nm, by about 30%, while at NA = 1.1, the contrast improves to about 30%, at the borderline of printability. Similarly, in Figure 3-9(b), for λ = 157 nm, we see that the consideration of annular illumination, in combination with liquid immersion and NA = 1.3, provides borderline printability for lines and spaces as small as 45 nm. Figures 3-10(a) and 3-10(b) show the corresponding DOF for the 193- and 157-nm situations, respectively. By comparing with Figure 3-8, we see that annular illumination provides a good improvement over pure circular illumination.

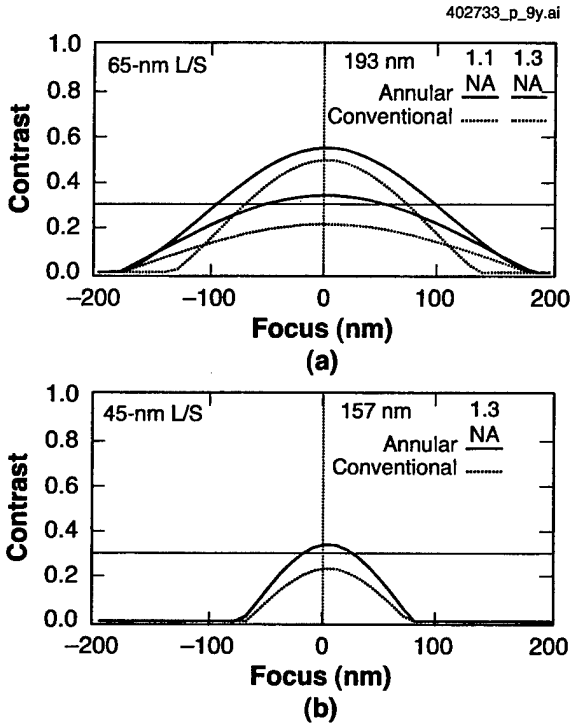

Figure 3-9. Comparison of contrast vs focus for annular (σ_{in} = 0.4, σ_{out} = 0.6) and circular (σ = 0.6) illumination: (a) 65-nm L/S, λ = 193 nm, and (b) 45-nm L/S, λ = 157 nm.

Similarly, if we use liquid immersion in addition to the well-known method of alternating PSM, which works well for alternating features of spaces and lines of equal size, we obtain results such as those illustrated in Figures 3-11 and 3-12. In order to take better advantage of the alternating PSM methods, a smaller partial coherence of 0.3 was used in these simulations. In Figure 3-11(a), we see that with alternating PSM, a very acceptable printability should be obtained for both dry and liquid immersion at λ = 193 nm, with NA as low as 0.9, for printing 65-nm lines and spaces; this represents a considerable improvement over a binary mask with circular illumination σ = 0.6, as in Figures 3-7(b) and 3-8(a). Still, of course, liquid immersion provides a larger process window, even for NA = 0.9. Moreover, with λ = 157 nm, as in Figure 3-11(b), we see that the use of alternating PSM plus liquid immersion produces a very acceptable DOF for printing lines and spaces as small as 45 nm at λ = 157 nm. Finally, Figures 3-12(a) and 3-12(b) show the DOF for various situations at λ = 193 and 157 nm, when the alternating PSM is used along with these very high NA applications.

The above analysis has also been generalized from simple contrast calculations, to exposure-defocus analysis, thereby enabling DOF predictions to be obtained for isolated structures, as well as more general

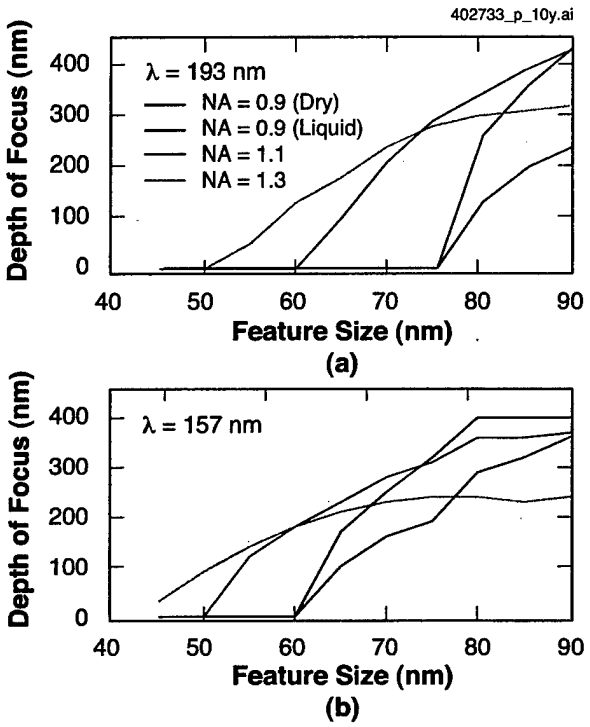

Figure 3-10. DOF vs focus for annular illumination (σ_i = 0.4, σ_{out} = 0.6): (a) λ = 193 nm and (b) λ = 157 nm.

one- and two-dimensional structures. Figure 3-13 illustrates the general idea. Figure 3-13(a) contains a plot of exposure vs focus for two situations: 75-nm lines and spaces exposed at 193 nm using a binary mask and circular illumination σ = 0.6 at NA = 0.9 (dry) and NA = 1.1 (liquid). The DOF improvement and general increase in process window are quite evident. For any given exposure latitude, Figure 3-13(a) can be used to calculate DOF, as shown in Figure 3-13(b). Comparing the 75-nm point in Figure 3-8(a), obtained via contrast calculations, we see excellent agreement with the 10% exposure latitude point in Figure 3-13. Finally, Figure 3-13(c) illustrates what happens if we push the technology using alternating PSM in addition to liquid immersion. As expected from the earlier contrast calculations, acceptable process windows look very feasible at 55-nm dimensions, with NA = 1.1 and 1.3 at λ = 193 nm.

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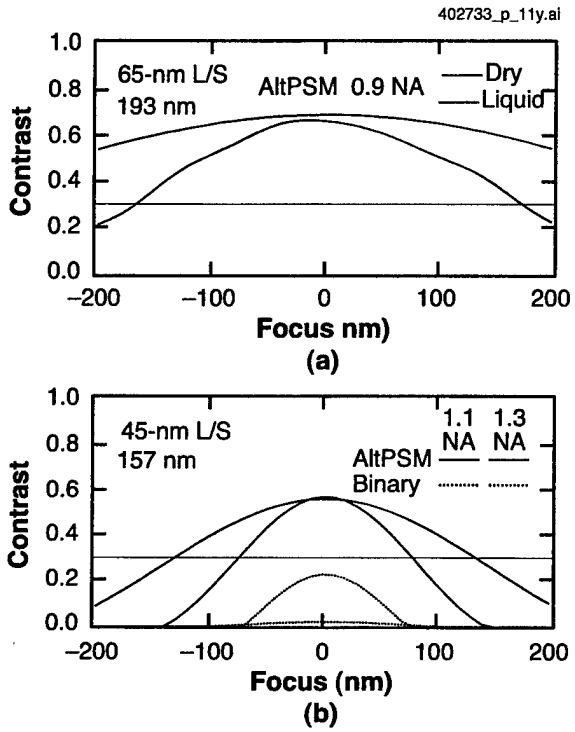

Figure 3-11. Comparison of contrast vs focus for alternating phase shift mask (PSM) ($\sigma = 0.3$) and binary mask ($\sigma = 0.6$): (a) 65-nm L/S, $\lambda = 193$ nm, and (b) 45-nm L/S, $\lambda = 157$ nm.

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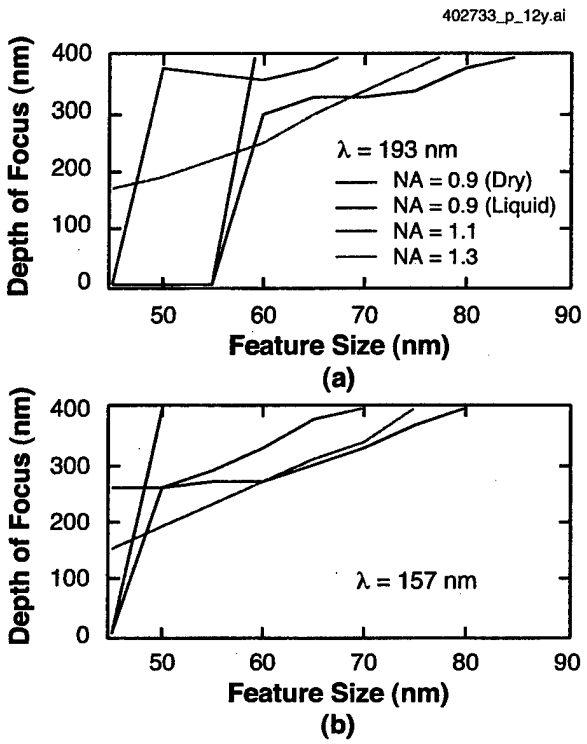

Figure 3-12. DOF vs feature size for alternating PSM (σ = 0.3): (a) λ = 193 nm and (b) λ = 157 nm.

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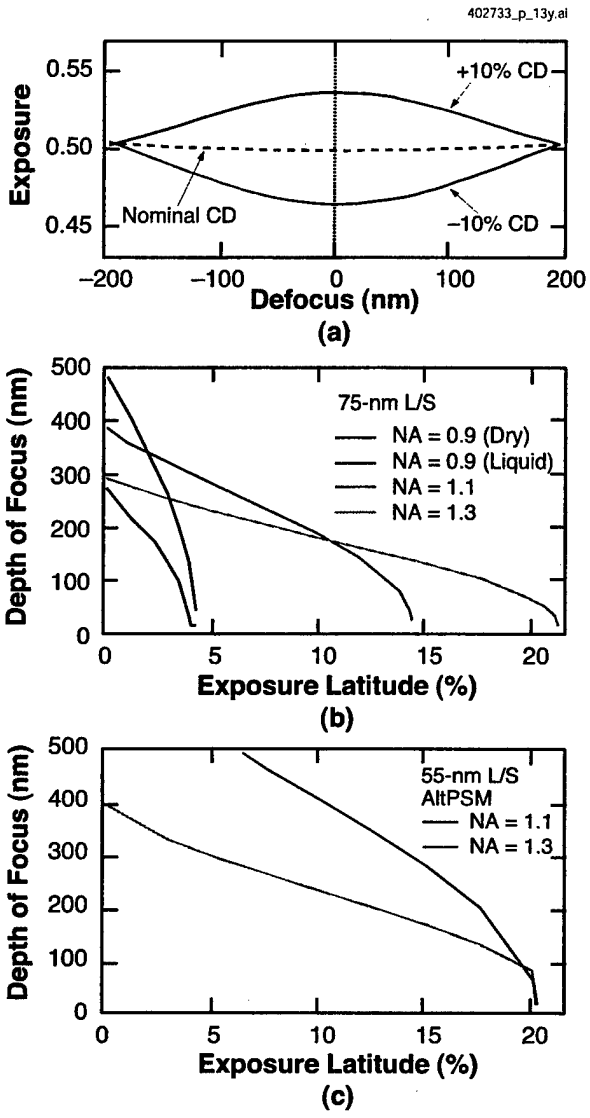

Figure 3-13. (a) Exposure-defocus plot for 75-nm L/S features at λ = 193 nm with binary mask, liquid immersion, and circular illumination (σ = 0.6) at a numerical aperture of 1.1. The dashed line represents the dose required to obtain the desired linewidth while the top and bottom curves represent the doses for ±10% variations in linewidth. (b) DOF vs exposure latitude (EL) for 75-nm L/S, λ = 193 nm, where EL is defined as the exposure difference between the ±10% lines, divided by the exposure at nominal printing. (c) DOF vs EL for 55-nm L/S, λ = 193 nm, using an alternating PSM and σ = 0.3 illumination.

4. BIOSENSOR AND MOLECULAR TECHNOLOGIES

4.1 TOXIN DETECTION WITH CANARY

The CANARY (Cellular Analysis and Notification of Antigen Risks and Yields) assay utilizes B cells that have been genetically engineered to produce aequorin, a calcium-sensitive bioluminescent protein originally found in the *Aequorea victoria* jellyfish [1]. We have genetically engineered B-cell lines that express antibodies specific for bacterial pathogens such as *Francisella tularensis* and *Yersinia pestis*. The B-cell detection system is intrinsically so fast (identification in <1 s) that the primary delay in the assay is the time required to bring the pathogens in contact with the B cells. We have solved this problem for agents large enough to be concentrated in a microcentrifuge by using a custom-built centrifuge integrated with a photomultiplier tube and a computer for signal readout. Data obtained for bacteria and large viruses (≥200 nm) using this centrifugation technique demonstrate excellent specificity as well as the best combination of speed and sensitivity of any known pathogen identification method. Although the current limit of detection is higher for small viruses (~50 nm) that cannot be concentrated with the centrifugation technique, we continue to investigate other approaches for bringing these agents into contact with the B cells.

Since CANARY successfully detects both bacteria and viruses, we believe the same system can be used for the detection of toxin antigens such as staphylococcal enterotoxin B, botulinum toxin, and ricin. The difficulty with detecting toxins is that while an antibody against a monomeric toxin expressed on the surface of B cells will bind to that toxin, each toxin molecule can only bind to one antibody. This binding fails to crosslink adjacent antibodies on the cell surface, as illustrated in Figure 4-1, and such crosslinking is required to generate the intracellular calcium flux and light emission. It is necessary, then, to modify the system such that toxin antigens are capable of crosslinking surface antibodies. There are two possible strategies to overcome this problem.

First, two antibodies, each specific for different epitopes on a toxin molecule (epitopes 1 and 2), can be expressed on the surface of the same B-cell line, as shown in Figure 4-2. The binding of a single toxin molecule to two antibodies (one antibody against epitope 1 and another antibody against epitope 2) crosslinks those two antibodies on the cell surface. Additional toxin results in additional antibody crosslinking and light emission. We have demonstrated that B cells are capable of expressing two functional antibodies simultaneously, by producing a cell line that expresses antibodies against both *Y. pestis* and *F. tularensis*. Each of these agents is recognized independently by this cell line, indicating that both antibodies are functional. This implies that it would be possible to generate two functional antibodies against different epitopes on the same toxin.

There are two indirect lines of evidence to indicate the potential sensitivity of CANARY to toxins. First, the cell line currently used to detect *Y. pestis* expresses antibody against the F1 antigen, a monomeric antigen that forms polymers in certain solutions. This antigen can be detected in its soluble, multimeric

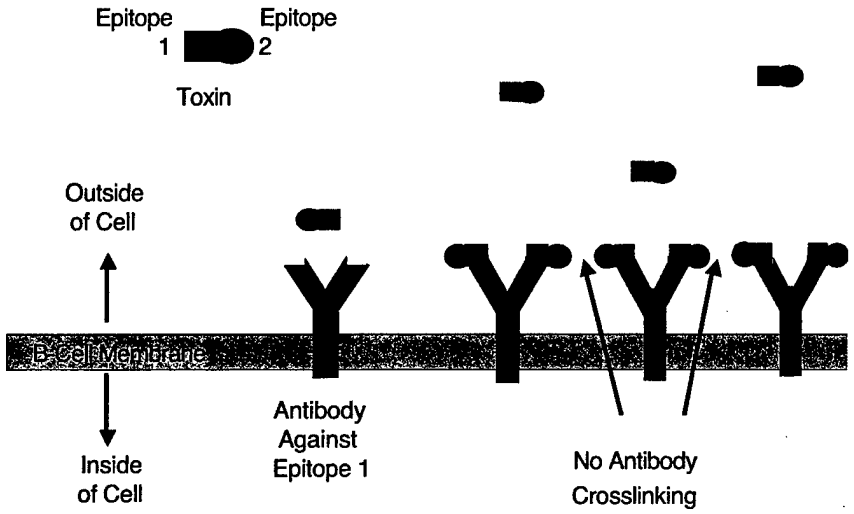

Figure 4-1. Antibody against epitope 1 of a given toxin is expressed on the surface of B cells. This antibody is capable of binding the toxin present in solution, but because the surface antibodies are not crosslinked, no signal is generated.

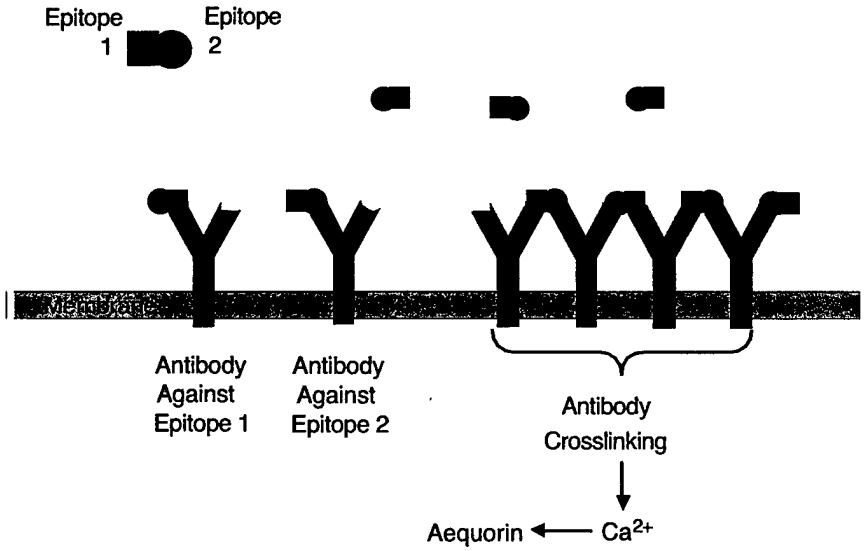

Figure 4-2. Single B-cell line is engineered to express two independent antibodies, each recognizing a different epitope on a single toxin molecule. The toxin is now capable of crosslinking the surface antibodies, resulting in increased intracellular Ca^{2+} and emission of light by aequorin.

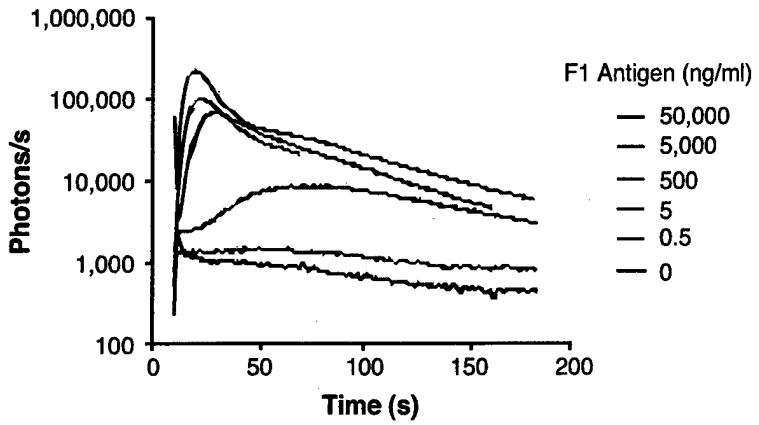

Figure 4-3. Dose response of the B-cell line expressing an antibody that recognizes the F1 antigen of Y. pestis, which exists in multimeric form in solution. Even without optimization of the assay, these data demonstrate excellent sensitivity to nonsedimentable antigen.

form by the B cells at concentrations as low as 5 ng/ml, as seen in Figure 4-3, which is approximately as sensitive as current immunoassay techniques. A second line of evidence that indicates the potential for toxin detection is drawn from experiments demonstrating detection of DNA. B cells expressing antibody against digoxigenin are used to detect digoxigenin-labeled oligonucleotides hybridized to DNA. In these experiments two oligonucleotides, each with a single digoxigenin label at the 5' end, are hybridized to each other. As seen in Figure 4-4, as little as 80 fmol of this soluble, double-stranded oligonucleotide with two attached digoxigenin molecules can be detected by CANARY cells. While the sensitivity of F1 polymer detection, digoxigenin-labeled DNA detection, and (theoretical) toxin monomer detection are only roughly analogous, these experiments demonstrate that CANARY can be quite sensitive to soluble agents. It should be noted that neither the soluble F1 nor the dsDNA detection have been optimized, and the ultimate sensitivity may be significantly better than shown.

We have clearly demonstrated that CANARY is excellent at detecting sedimentable antigens containing multiple copies of a given epitope. An alternative, or possibly complementary, approach to the toxin detection strategy outlined above would be to express one of the toxin antibodies on the surface of a benign bacterial strain and the second antibody on the surface of B cells, as illustrated in Figure 4-5. In the presence of toxin, the surface of the (killed) bacteria will be decorated with toxin. These toxin-bound bacteria could be sedimented by centrifugation, and B cells expressing the second antibody added. Because the soluble toxin antigen is immobilized on the surface of bacteria, the B-cell toxin antibodies would be crosslinked, would initiate the signal transduction, and would activate aequorin. Our research clearly shows the detection of bacterial surface antigens and the increased sensitivity resulting from

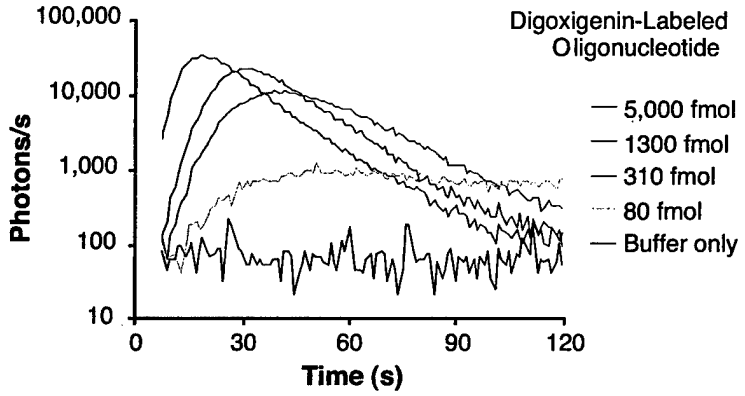

Figure 4-4. Two complementary oligonucleotides, each labeled with digoxigenin, were hybridized and various amounts used to challenge CANARY cells. The limit of detection in this assay was 80 fmol.

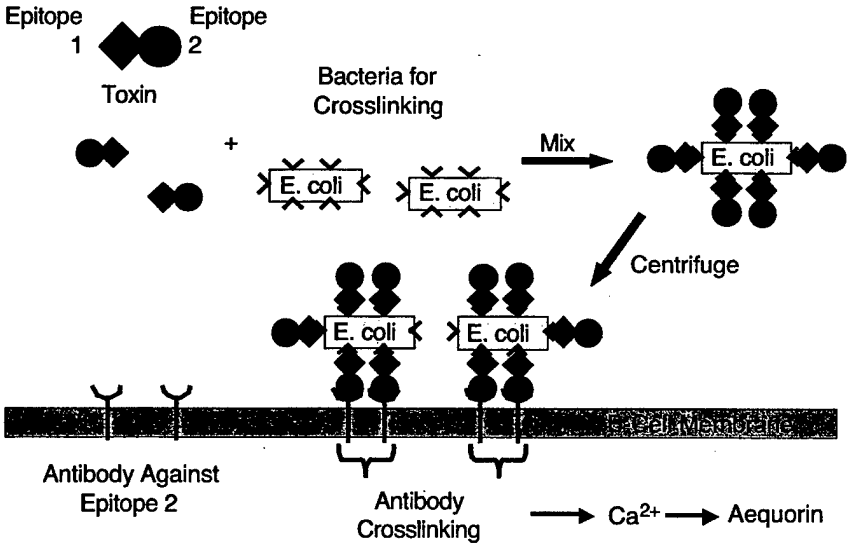

Figure 4-5. Antibody against epitope 1 of a toxin is expressed on the surface of bacteria. Soluble toxin binds to these antibodies, coating the bacteria with toxin antigen. These toxin-coated bacteria are sedimented by centrifugation prior to addition of B cells expressing antibody against epitope 2. Crosslinking of the B-cell antibodies results in light emission by aequorin.

sedimenting those bacteria prior to the addition of B cells. This alternative approach would capitalize on the increased sensitivity of CANARY to sedimentable antigens.

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5. ADVANCED IMAGING TECHNOLOGY

5.1 CHEMISORPTION-CHARGING PROCESS FOR BACK-ILLUMINATED IMAGE SENSORS

Silicon detectors operating in the regime of photon energies from 3 to 500 eV face the problem of surface recombination losses because of the shallow (<500 nm) photon absorption lengths. These losses reduce the quantum efficiency of the device. For soft-x-ray detectors operated in a spectroscopic mode, the photoelectron loss degrades the energy resolution of the device. The challenge is to develop a surface passivation treatment that results in low surface-recombination losses and is compatible with the device processing. Recently we began collaborating with the University of Arizona Imaging Technology Laboratory to apply a surface treatment developed there, termed chemisorption charging [1], to our back-illuminated charge-coupled devices (CCDs). This process has been shown to produce low recombination losses and high quantum efficiencies in the visible and ultraviolet spectral regions. Here, we describe results from devices with this treatment tested as soft-x-ray detectors.

We have employed a number of techniques over the past decade to try to achieve a soft-x-ray detector with high quantum efficiency and good energy resolution. In all cases, the process must be applied to back-illuminated CCDs, since the dielectric and polysilicon layers comprising the CCD gates are too absorptive. This places major constraints on the process options that can be used. The most successful of these was the so-called refractory process in which the back surface of a chemically thinned CCD wafer was oxidized at high temperatures, then implanted with boron and annealed to activate the implant [2],[3]. The oxidation ensured a low surface-state density for reduced surface recombination, and the boron provided a repulsive field for photoelectrons. The process was somewhat difficult to perform, since it involved various process steps, including the final metal deposition and lithography, on a thinned, free-standing wafer. Although the quantum efficiency and energy resolution were regarded as excellent, the device yield was very low. In addition, the charge-transfer inefficiency (CTI) was higher after the process ($\sim 10^{-5}$) than before (10^{-7}–10^{-6}), though still in an acceptable range. The two back-illuminated CCDs on the Chandra mission were treated with the refractory process.

Other back-surface treatments include an ion implant followed by pulsed laser anneal [4]. This process produces a p^+ doped region about 100 nm deep but does not leave a well-passivated surface. A significant fraction of the photoelectrons absorbed within the 100-nm p^+ layer are lost to recombination, and as a result this process works well only for photons that have absorption lengths >>100 nm. More recently, we have explored molecular beam epitaxy (MBE), which can produce p^+ layers of order 5-nm thickness. Although optical data showed excellent quantum efficiency in the UV at room temperature [5], results at temperatures below –50°C, where x-ray astronomy missions typically operate, showed variable results. We believe that in some instances shallow traps in the MBE layer reduced the negative space charge that is critical to repelling photoelectrons from the surface.

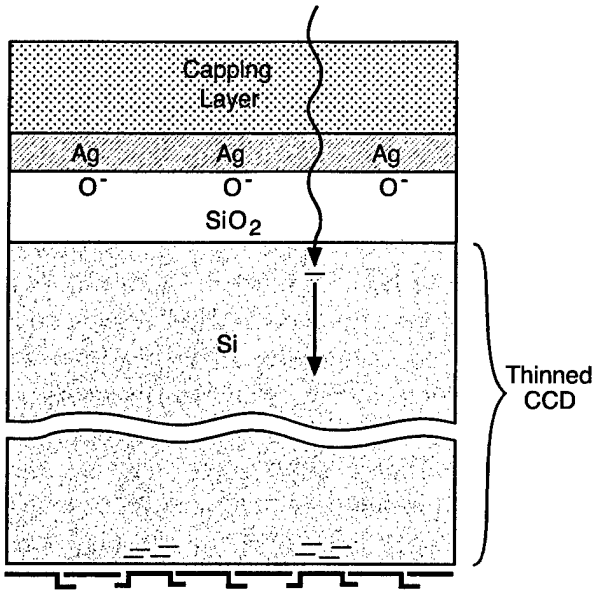

Figure 5-1. Depiction of cross section of silicon image sensor treated with the chemisorption-charging process.

The chemisorption-charging process has been applied to UV/visible detectors, but until now it has not been evaluated for soft-x-ray detectors. It is a simple, low-temperature process with high yield. Figure 5-1 depicts in cross section the key features of the resulting CCD. The thinned device wafer is first oxidized in H_2O and O_2 at 130°C at a pressure of about 40 psi for a period of 24 h. This produces a layer of about 3-nm SiO_2, which reduces the surface-state density and allows some bending of the energy bands at the surface. A 1-nm layer of Ag is deposited, followed by a capping layer to protect the Ag from chemical attack during subsequent processing and storage. For the devices used in the x-ray measurements the capping layer was 80 nm of HfO_2, which was chosen as an antireflection coating for the originally intended use as UV/visible detectors. Silver (as well as copper) will dissociate oxygen and lead to the formation of O^- ions that provide the repulsive field needed to keep photoelectrons away from the Si/SiO_2 interface.

X-ray data from a chemisorption-charged CCD at the oxygen and carbon Kα lines are shown in Figures 5-2 and 5-3. The device was made on 4000-Ω-cm *p*-type silicon and had 15-μm pixels. The data were taken with the device at –90°C and with clock voltages to fully deplete the 45-μm-thick device. Shown for comparison are data at the same energies from devices with the refractory process. The x-ray resolution of the chemisorption-charged devices is somewhat better (ΔE = 122 and 111 eV full width at half-maximum) than that of the refractory CCDs (ΔE = 127 and 114 eV), as well as being superior to that of the laser-anneal and MBE-processed devices [5]. In addition, the CTI remained at ~10^{-6} before and after processing, in contrast to the refractory process. One handicap of the chemisorption-charged devices in

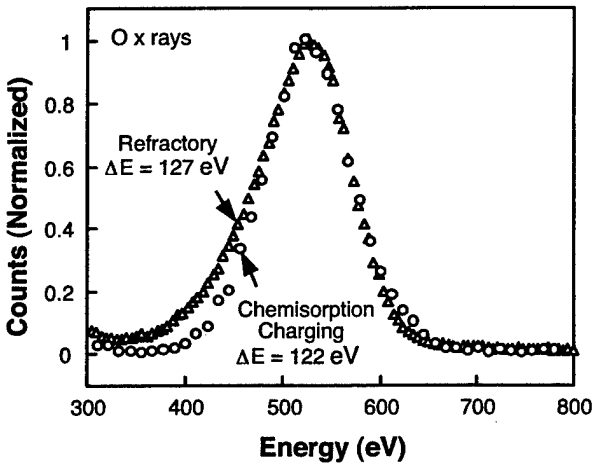

Figure 5-2. X-ray response at the oxygen K line (525 eV) for devices treated with refractory and chemisorption-charging processes.

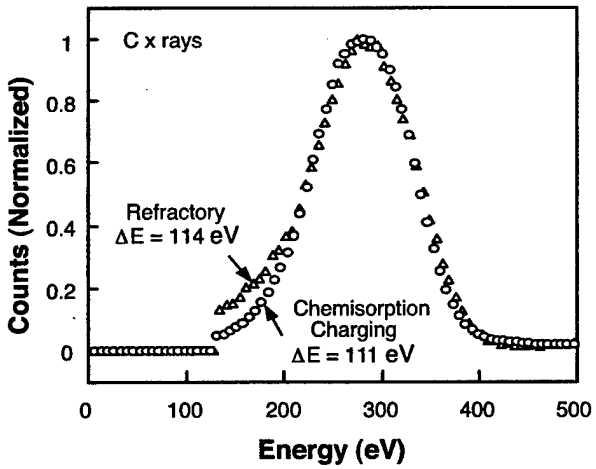

Figure 5-3. X-ray response at the carbon K line (277 eV) for devices treated with refractory and chemisorption-charging processes.

these experiments is their smaller pixel size of 15 μm, compared to 24 μm for the Chandra refractory-processed devices. The smaller pixel size leads to more split events, which tends to degrade ΔE. It is likely, therefore, that better resolution can be obtained with this new process if the CCD is either made thinner or with larger pixels.

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6. ANALOG DEVICE TECHNOLOGY

6.1 DESIGN OF A COUPLED TWO-QUBIT QUANTUM COMPUTER ELEMENT

As described previously, a Type-II quantum computer (T2QC) comprises an array of small, independent quantum computers with classical data communication between them [1]. The two fundamental units in each quantum computer module are (1) a qubit together with the circuitry to set up its initial state (before the qubits are caused to interact to perform the computation) and to read out its final state after the computation, and (2) a circuit to provide controlled coupling between pairs of qubits.

The theory behind the operation of a qubit unit has been described, along with some experimental measurements on the sensitivity of a quantum flux parametron (QFP) readout circuit [2]. That QFP was of an earlier design; here, we present the newest design approach, which takes into account a number of factors that are important in a quantum environment. These designs (1) eliminate resistors with their associated Johnson noise, which induces decoherence of the qubit states; (2) implement as precise symmetry as possible to maintain orthogonality between modes that we do not want to interact; and (3) minimize stray magnetic fields and ground-plane currents to prevent unwanted coupling between signals.

Figure 6-1 shows the layout of a qubit unit. The persistent-current qubit is at the lower right, where one of its sides overlaps—and inductively couples to—the spine of the QFP. The superconducting quantum interference device (SQUID) for reading out the latched state of the QFP is at the lower left, where one of its sides also overlaps and inductively couples to the spine.

One new feature of the design is that, whenever possible, wires that bring in control signals have separate return wires, and those return wires overlap the signal wires. This approach minimizes stray magnetic fields and interactions via ground-plane currents. For example, consider the bias line at the lower right that applies a magnetic flux bias to the qubit. The bias current enters on an M2 wire (red), runs over the lower qubit arm to couple in the flux, exits from the qubit, flows through a via to a wire in layer M4 (black), and then runs back out directly on top of the incoming M2 wire. The same technique is used for the QFP exciter (marked EXC in the figure) and for the SQUID bias and SQUID readout (marked R/O). The QFP offset bias is the sole exception. Its current divides among three paths (the two QFP arms and the QFP spine) and returns via the common ground plane and a wire connected to the ground plane off the figure to the right. Here, the ground plane is a necessary part of the circuit.

A second new feature is the topological configuration of the QFP. In conventional superconductive electronic circuits, the exciter arms run straight across, forming a "T" with the spine. In the new design we have folded the arms upward (1) to get the exciter current as far from the qubit as possible and (2) to get the junctions, which inject their current into the ground plane, close together and away from the qubit. Furthermore, in conventional implementations of the QFP, the exciter current enters on one side and exits on the other. Here, we have folded the exciter wiring back next to itself to reduce stray magnetic fields generated by the large exciter current.

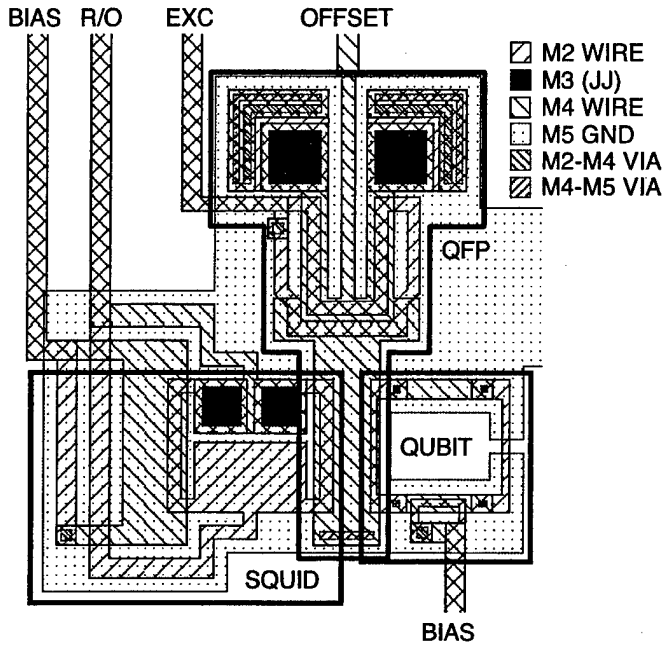

Figure 6-1. Layout of basic qubit circuit, comprising the qubit itself plus the quantum flux parametron (QFP) detector, which includes a superconducting quantum interference device (SQUID) to sense the state of the QFP. For scale, the squares in the legend at the upper right are 3 μm on a side.

A third change is the use of a symmetric SQUID rather than the usual asymmetric SQUID for reading out the QFP. Since a symmetric SQUID can not distinguish between spine currents of equal magnitude but opposite direction, one must provide a way to introduce an asymmetry when the SQUID is operated. This is accomplished by the external bias line, which puts the degree of asymmetry under external control and allows it to be optimized during operation. Note that this bias will be applied after the QFP has already been fired, at which point disturbance of the qubit state is no longer a concern.

We now turn our attention to the circuit for introducing an electrically controllable coupling between two qubits. The basic principle is illustrated in Figure 6-2(a). The currents in the two qubits are coupled magnetically via a loop of wire between them, and the magnitude of the coupling is controlled by varying a series inductor in the loop. The larger the series inductor, the smaller the coupling. In order to handle both positive and negative coupling and to make it possible to set the coupling to zero, two loops are used, as shown in Figure 6-2(b), one of which has one of its coupling inductors reversed. If the two loops have identical inductances, then the net coupling will be zero. Increasing the series inductance in one of the loops will reduce the coupling caused by that loop, allowing the coupling introduced by the other loop to dominate. (Filippov et al. [3] have independently reported a circuit based on the same principles.)

Figure 6-3 shows the complete schematic for the coupling circuit, including the SQUID loops that implement the variable series inductors. Figure 6-4 shows the actual layout of the circuit. A Josephson junction carrying a bias current I_B acts, for small variations in that current, like an inductor with an inductance L_J given by

$$L_J = \left(\frac{\Phi_0}{2\pi}\right)\left(\frac{1}{\sqrt{I_C^2 - I_B^2}}\right) \tag{6.1}$$

where Φ_0 is the flux quantum ($\sim 2 \times 10^{-15}$ Wb) and I_C is the junction critical current. As the bias current increases, the effective inductance grows and approaches infinity as the bias current approaches the critical current.

Note that the inductance value does not depend on the sign of the bias current; current in either direction raises the effective inductance of the SQUID loop and reduces the qubit-qubit coupling via that coupling loop. Thus, to create positive coupling, bias current must be applied to one SQUID, while negative coupling requires the application of bias current to the other SQUID. For perfectly matched components, applying currents of equal magnitude to both control inputs will leave the total coupling between qubits at zero.

The balanced design of this coupling circuit is crucial to its operation. The purpose of the circuit is to induce controlled coupling between the two qubits, and only between the qubits. We do not want any coupling of the control currents to the qubits. By making the control current couple symmetrically into each side of the SQUID loop, as shown in Figure 6-3, the bias current induced in the SQUID loop by the control current will be confined entirely to the SQUID loop; none will flow through the coupling loop itself and create a shift in the flux bias applied to the qubits.

The layout of the circuit, shown in Figure 6-4, very carefully preserves symmetry between the two coupling loops so that the coupling will be zero when no control currents are applied and when the components match perfectly. Parasitic inductance in the loops, which reduces the dynamic range of the coupling, was minimized by using wide lines where possible. As in the qubit circuits, control current lines have their own individual return lines running congruently to minimize stray magnetic fields.

In any real circuit, of course, the component values—the junction critical currents and the self and mutual inductances—will not be perfectly matched. As a result, two problems will arise. First, with no control currents applied, there might still be some coupling between the two qubits owing to a mismatch between the two coupling loops. Second, the control currents will couple directly to each of the qubits owing to mismatches within the SQUID loops. Fortunately, we have enough degrees of freedom in the circuit to compensate for such mismatches, in case they are large enough to affect performance. We will consider two examples to illustrate the possibilities for each of these problems.

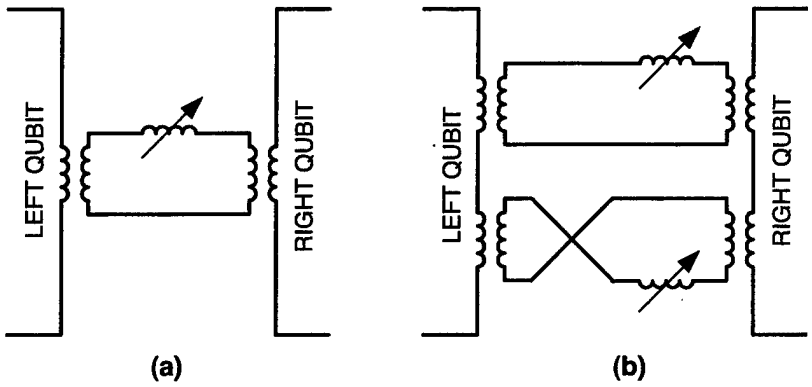

Figure 6-2. Diagrams illustrating the principles behind the qubit coupling circuit. The basic principle is to couple flux between the qubits via a loop of wire with a variable series inductor, as shown in (a). The coupling decreases as the variable series inductance increases. Using a pair of coupling loops, as shown in (b), with one coupling inductor wired in reverse, creates a balanced circuit that can provide a coupling factor that spans a bipolar range and produces zero net coupling when the series inductors are the same.

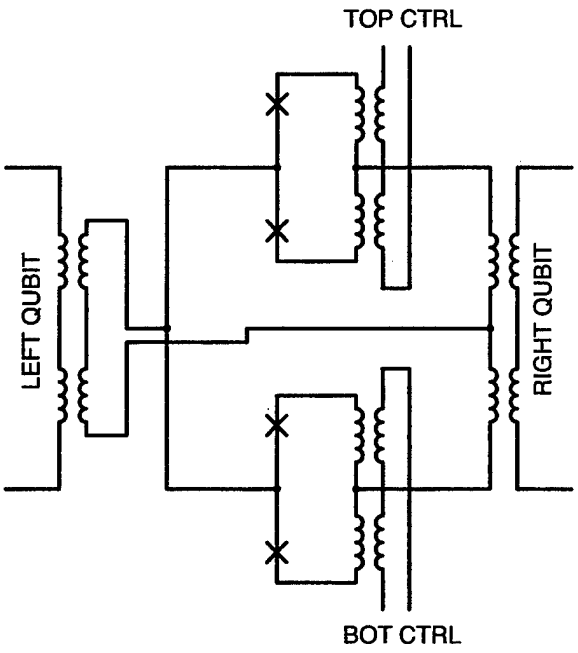

Figure 6-3. Complete schematic for the electrically controllable coupling circuit. A loop with two Josephson junctions provides the variable inductance. The critical currents of those junctions are much larger than the currents induced by the qubit currents, and they, therefore, act like inductors. When control current is applied, a circulating current in the junction loop causes the effective junction inductance to increase, reducing the coupling between qubits.

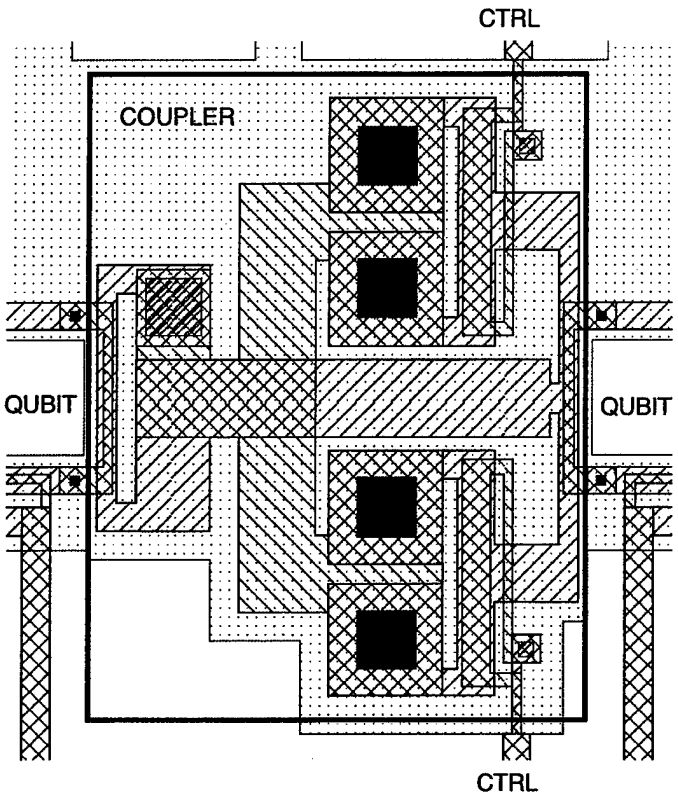

Figure 6-4. Coupler circuit between two qubits. The qubit on the right is part of the circuit shown in Figure 6-1, while the qubit on the left is its mirror image. The coupler creates an effective mutual inductance between the two qubits that ranges from negative to positive. With no current in either control line, the symmetry of the coupler leads to zero coupling.

Regarding the first issue, let us assume that all components are perfectly matched except that the two Josephson junctions in the top SQUID have a higher critical current—and thus lower effective inductance—than the two junctions in the bottom SQUID. We can then compensate for the higher coupling provided by the top loop by maintaining a higher control current to that loop than would otherwise be needed to achieve the desired net coupling between the qubits (and a nonzero bias to achieve zero coupling).

The second issue is more complex. Let us assume that all components are perfectly matched except that in the top SQUID the two junctions have different critical currents, one a little larger than the target value and one correspondingly smaller. The two coupling loops will still match exactly with zero control inputs, but when a control current is applied to the top SQUID to induce coupling between the qubits, some of the circulating bias current in the top SQUID will flow through the coupling loop and shift the net flux

bias applied to each qubit. The total qubit flux biases can be maintained at their proper, constant values by simultaneously adjusting the direct biases to each qubit (via the lines labeled BIAS in Figure 6-1).

Finally, the quantum nature of the circuits adds special concerns to the design. In the discussion above we treated the coupling circuit as a purely classical system. In fact, it is critical that the coupling circuit not have multiple quantum states that could be excited during normal operation and become entangled with the qubit states. The best way to avoid such entanglement is to be sure that the qubit's field does not affect the coupling circuit's ground state. We have calculated this effect and shown that it is insignificant for the circuit parameters chosen. The junctions in the coupling circuit have much higher critical current values—and thus greater effective mass—than the junctions in the qubits, and this keeps entanglement between the two circuits in check.

The designs described here have been fabricated as part of what we called the QC4 multiproject run, which has now been completed. In addition to the full circuits shown in Figures 6-1 and 6-4, we included test circuits for evaluating individual design elements. One such circuit comprises the coupling circuit shown in Figure 6-3 but with an external direct input of current in place of the right-hand qubit and a QFP current detector to directly measure the current induced in the left qubit. Thus, we will be able to study and characterize the coupling circuit directly. We expect to report on the experimental results in a future issue.

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7. ADVANCED SILICON TECHNOLOGY

7.1 SUBSTRATE REMOVAL AND BOX THINNING EFFECTS ON TOTAL DOSE RESPONSE OF FDSOI nMOSFET

Thin-film fully depleted silicon-on-insulator (FDSOI) technology has recently emerged as one of the preferred approaches for advanced CMOS field-effect transistor (FET) scaling [1]. As in bulk silicon CMOS, ionizing radiation induces a negative shift of the transistor threshold voltage, thus increasing *n*-channel FET (nFET) leakage current. In submicron processes, the gate oxide is so thin that it contributes very little to the transistor threshold voltage shift. Instead, threshold shifts are caused by charge trapping in the lateral isolation oxide and the buried oxide (BOX) [2],[3]. Charge trapping in the isolation oxide, which can be either a local oxidation of the silicon, a deposited oxide in a trench, or an oxide on a mesa sidewall, can cause a parasitic edge leakage [2]. Using an FET layout with no edge can mitigate this problem, but such transistors are larger and dramatically increase the circuit size, which can limit circuit performance and prevent scaling and reuse of circuits from existing non-radhard circuit libraries. Ionizing radiation effects in the BOX are also challenging because in fully depleted transistors, the BOX is coupled to the front channel [4]. Some tolerance to ionizing radiation has been demonstrated with special oxide treatments applied to either the isolation oxide or the BOX [3], though additional treatment optimization and circuit validation are required. Double-gate and gate-all-around transistors are expected to alleviate problems associated with thick oxides [5], but further development in those fabrication techniques is still required for meaningful radiation studies.

Results presented here show that our new FDSOI mesa isolation is effective in suppressing edge-induced leakage current before and after total dose irradiation, unlike our previous process generations [2]. Analytical modeling of experimental test data further demonstrates that radiation-induced shifts are caused solely by charge trapping in the BOX. We previously demonstrated that a significant enhancement in the total dose radiation response of 0.25-μm, 2-V, FDSOI FETs was obtained after substrate removal [6]. Since then, we made some improvements to the fabrication techniques and have duplicated the earlier experiment on 0.18-μm FDSOI CMOS wafers. We also show new results after substrate removal and BOX thinning.

Here, we present the results, analysis, and modeling of the total dose radiation effects in 0.18-μm, 1.5-V, FDSOI nFETs on standard SOI wafers. We show that a one-dimensional model fits well the experimental data for different device layout and bias conditions during irradiation. Then, we report new radiation effects on the FDSOI FETs after substrate removal and thinning of the BOX from 200 to 56 nm. Radiation effects in FDSOI *p*-channel FETs are not discussed.

FDSOI transistors and circuits were fabricated on Lincoln Laboratory's 0.18-μm, 1.5-V, FDSOI CMOS process on standard Unibond wafers with 200-nm-thick BOX. The silicon substrate below the BOX is *p* type with a resistivity between 1 and 10 $\Omega \cdot$cm. Capacitance-voltage (C-V) curves show that the silicon

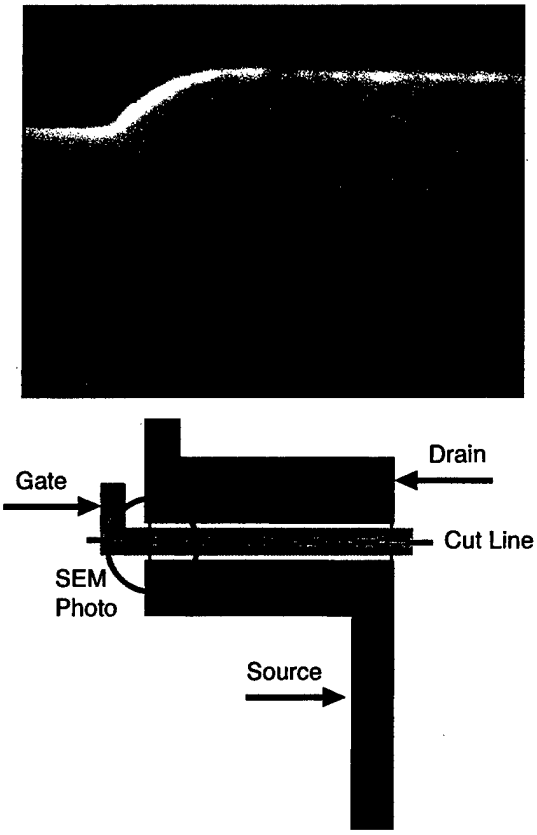

Figure 7-1. Photograph of cross section of mesa-isolated fully depleted silicon-on-insulator (FDSOI) field-effect transistor (FET) on Unibond wafer taken with a scanning electron microscope.

under the BOX is typically depleted or weakly inverted in normal operating conditions. The process flow includes mesa isolation, 40-nm-thin SOI islands, 4.2-nm gate oxide, 0.18-μm FET minimum gate length, silicon nitride spacers, moderately doped source drain extensions, cobalt salicided source/drain/gate, dual-doped polysilicon gates, and a fully planarized 3-metal level back end with tungsten plugs [7]. The photograph in Figure 7-1 shows the cross section of an FET mesa island taken on a scanning electron microscope. Our optimized mesa isolation process minimizes BOX etching near the island edge, unlike our earlier process [2]. It prevents the poly gate from wrapping around the SOI islands and, along with an edge implant, minimizes parasitic edge leakage. Over 150 circuits have been fabricated with this process as part of DARPA-funded FDSOI multiproject runs for 30 different government, industry, and academic organizations. Circuit applications included low-power digital and mixed-signal applications.

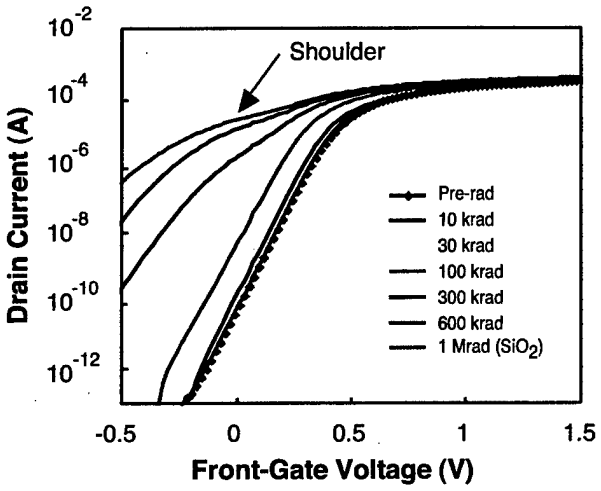

Figure 7-2. Front-gate semilogarithmic current-voltage (I-V) curves at 50-mV drain bias with the back gate at 0 V for a W = 8 μm, L = 0.18 μm FDSOI nFET on Unibond wafer with 200-nm buried oxide (BOX).

The total dose radiation response of nFETs was characterized at various total dose increments up to 2 Mrad (SiO_2) on an Aracor 4100 equipped with a 10-keV tungsten x-ray source; 1 Rad (SiO_2) is equivalent to 1.8 Rad (Si). The dose rate was between 10 and 100 krad (SiO_2) per minute. The exposure time was between 0.7 and 5 min depending on the dose increment. The nFET bias during irradiation was offgate, that is, with the drain biased at 1.5 V, or ongate, that is, with the gate biased at 1.5 V, with all other terminals grounded in both bias conditions. Drain current vs front- and back-gate voltage current-voltage (I-V) curves were acquired under computer control on an HP4155B parameter analyzer approximately 30 seconds after irradiation was stopped. All testing was done at the wafer level.

Figures 7-2 and 7-3 show typical front-gate semilogarithmic and linear I-V curves, respectively, with 50 mV on the drain for an L = 0.18 μm mesa nFET irradiated in the offgate bias condition. Pre-radiation, the I-V curve exhibits no shoulder with a nearly ideal subthreshold slope of 65 mV/dec, indicating that our optimized mesa isolation is effective in suppressing parasitic edge leakage. For doses greater than 100 krad (SiO_2), the front-gate subthreshold leakage current exhibits a shoulder when the front-gate voltage is around 0 V. This shoulder was present on all the front-gate I-V curves regardless of the transistor layout, including H-gate and annular devices in which no edge channel is possible. (With an annular gate, the transistor literally has no edges. In plan view an H-gate is in the shape of an H, with the channel under the crossbar and body contacts outside the two uprights. Thus the "edges" where the gate leaves the active region are diodes, not parasitic transistors.) We will show that the shoulder is due to back-channel current. Figures 7-2 and 7-3 also show that the radiation-induced shift in the subthreshold region is much larger than at high drain current. The threshold voltage shift, ΔV_{TF}, at 50-mV drain bias and extrapolated from the voltage at maximum transconductance, is –0.3 V at 1 Mrad (SiO_2). There is no loss

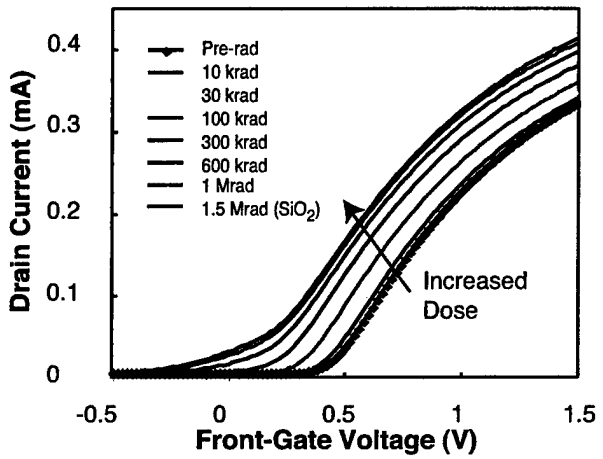

Figure 7-3. Front-gate linear I-V curves at 50-mV drain bias with the back gate at 0 V for a W = 8 μm, L = 0.18 μm FDSOI nFET on Unibond wafer with 200-nm BOX.

in transconductance up to 1.5 Mrad (SiO_2) even at high current. Figure 7-4 shows that the back-gate I-V curves pre- and post-irradiation exhibited two distinct subthreshold slopes, above and below ~5 nA. These curves were quite similar for all transistor layouts. We noted that on the front- and back-gate I-V curves, the radiation-induced shift seems to saturate at a total dose of about 1 Mrad (SiO_2).

To understand the shoulder of Figure 7-2 we consider first the back-gate characteristic of Figure 7-4. It shows two different subthreshold slopes for all radiation doses. The steeper slope, at higher current, is labeled back, and the shallower slope at lower current is labeled front. The two-dimensional (2D) Atlas [8] device simulation of Figure 7-5 reveals the source of the two slopes. At relatively high back-gate voltage, on the steeper part of the curve (C in Figure 7-5), the simulation shows electron concentration in the back channel ~10× higher than in the front channel. So at high current in Figure 7-4, the current flow is dominated by the back channel. At relatively low back-gate voltage (A in Figure 7-5), the electron concentration in the back channel is >100× lower than in the front channel. So at low current in Figure 7-4, the current flow is dominated by the front channel. The subthreshold slope in that region is less steep simply because the front channel is farther away from the back gate than is the back channel.

Comparing Figure 7-4 with Figure 7-2, we see that at 0 V on both gates and a dose of 100 krad (SiO_2) or below, the current is dominated by the front channel. At a dose of 300 krad (SiO_2) or above, the current is dominated by the back channel. This back channel current clearly causes the shoulder at high doses in Figure 7-2. This explains why shoulders appear after irradiation in both edge and edgeless transistors.

Next, we consider the magnitude of the threshold shift, measured at currents well above the shoulder region. We make the hypothesis that the threshold shift is caused entirely by charges in the buried oxide,

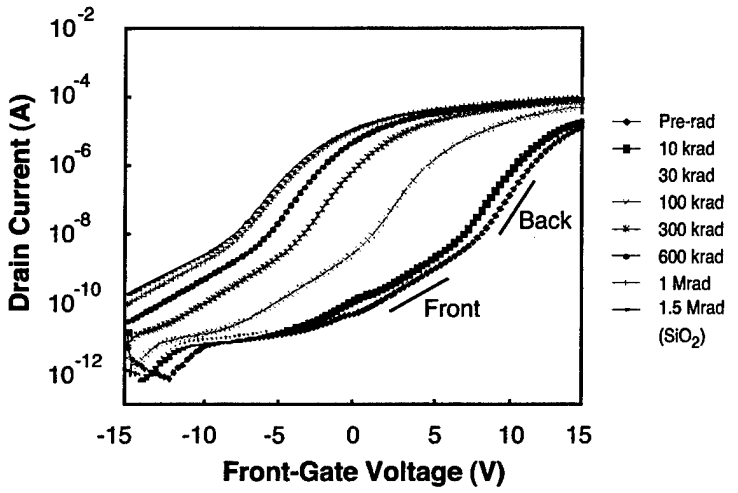

Figure 7-4. Back-gate semilogarithmic I-V curves at 50-mV drain bias with the front gate at 0 V for a W = 8 μm, L = 0.18 μm FDSOI nFET on Unibond wafer with 200-nm BOX. Front and back refer to the main conduction channel at the front and back gates, respectively.

and show that this hypothesis is consistent with the data. If charges in the thin gate oxide [3] do not play a major role in the radiation response, then one should be able to predict the threshold voltage shift of FDSOI transistors vs total dose solely considering radiation-induced charge trapping in the BOX. To verify this, we used the front-to-back channel coupling model of Lim and Fossum [4] to estimate the front-channel threshold shift, ΔV_{TF}, from the shift in the back-gate I-V curve, ΔV_{TBack}. This one-dimensional model assumes that the SOI body is fully depleted, the fixed oxide and interface charges are located at the SOI/oxide interfaces, the drain bias is low, and there is no depletion in the substrate or the polysilicon gate. The shift in the back-gate I-V curve with dose, ΔV_{TBack}, was calculated from data such as those in Figure 7-4 but for a front-gate voltage of –0.5 V so that the drain current was dominated by back-channel current over several decades. The variation in the BOX radiation-induced net charge density, ΔQ_{NET}, was extracted at each total dose increment from the back-gate voltage shift, ΔV_{TBack}, as follows:

$$\Delta Q_{NET} = C_{BOX} \times \Delta V_{TBack} \tag{7.1}$$

where $C_{BOX} = \varepsilon_{ox} / t_{BOX}$ is the BOX capacitance. The front-gate V_{TF} shift, ΔV_{TF}, was then calculated from the Lim and Fossum equation,

$$\Delta V_{TF} = -C_{Si} / \left[C_{OF} \left(C_{Si} + C_{BOX} + C_{IT} \right) \right] \times \Delta Q_{NET} \tag{7.2}$$

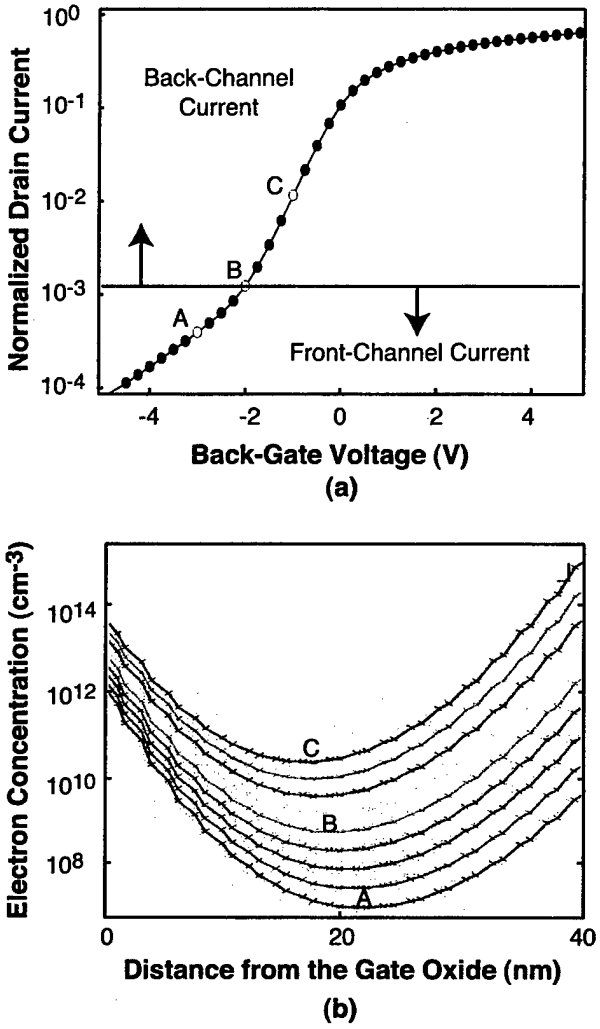

Figure 7-5. (a) Two-dimensional Atlas simulations of back-gate I-V and (b) electron concentration (electrons per cm^{-3}) in the SOI body with the front gate at 0 V. A, B, and C correspond to a specific back-gate voltage where the electron concentration is, respectively, largest at front channel, equal at front and back channels, and largest at the back channel.

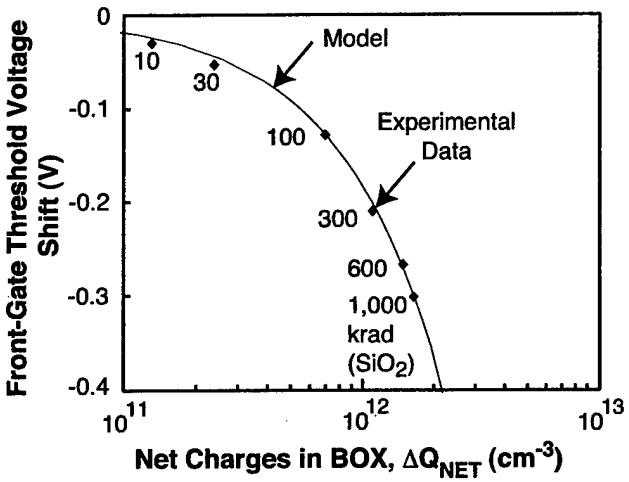

Figure 7-6. Experimental and modeling results of front-gate threshold voltage shift vs the net charges in the BOX, ΔQ_{NET}, for W = 8 μm, L = 0.18 μm FDSOI nFET in the offgate bias during irradiation. The experimental data points are labeled with the total dose from which they were extracted.

where $C_{Si} = \varepsilon_{Si}/t_{Si}$ is the capacitance of the depleted SOI layer. C_{OF} is the front-oxide capacitance, a function of the front-gate oxide thickness, and $C_{IT} = qN_{IT}$ is the capacitance due to interface traps at the SOI/BOX interface of density N_{IT}, with q being the electron charge. In this analysis, we set C_{IT} to zero.

At each total dose increment, experimental values of ΔV_{TF} were determined by extrapolation from the point of maximum transconductance on the front-gate I-V of $L = 0.18$ μm nFETs. ΔV_{TF} calculated with Equation (7.2) (and $C_{IT} = 0$) and experimental ΔV_{TF} are plotted together in Figure 7-6 vs ΔQ_{NET}. Simulated and experimental results agree quite well, thus confirming that radiation-induced shifts in the $L = 0.18$ μm FDSOI mesa nFETs are entirely caused by positive charge trapping in the BOX.

ΔQ_{NET} appears to saturate at about $+1.8 \times 10^{12}$ cm^{-2} at 1.5 Mrad (SiO_2), which is consistent with values reported by others on a similar FDSOI CMOS process [9]. We noted that the back-gate subthreshold slope and the back-gate transconductance did not change substantially up to 2 Mrad (SiO_2). We interpret this as an indication that the interface trap density at or near the BOX-SOI interface does not substantially increase since the negative charges in these traps may contribute to the saturation of ΔQ_{NET}. The front-gate transconductance above threshold did not change significantly with total dose (<5%), also indicating that little or no contribution from radiation-induced traps at the front-gate oxide occurs even at doses up to 2 Mrad (SiO_2).

Thus, we have shown that in our FDSOI nFETs on standard SOI wafers, the front-gate threshold shift is solely caused by radiation-induced charges in the BOX. One might expect that removing the substrate or thinning the BOX would change that charge trapping. We did experiments to explore this

question. Indeed, we observed that ionizing radiation effects changed significantly when the silicon substrate was removed below the BOX of an FDSOI FET.

Substrate removal and BOX thinning were carried out using our oxide-based wafer-to-wafer bonding process, which is described in detail elsewhere [10]. Briefly, a layer of low-temperature oxide (LTO) was deposited on the completed FDSOI wafer and on a mating carrier wafer. The LTO was polished by chemical-mechanical polishing to achieve a surface roughness of ~0.4 nm rms. The wafers were cleaned in H_2O_2 at 80°C for 10 min, rinsed, spun dry, and bonded at room temperature. A 10-h, 275°C thermal cycle was used to increase the bond strength sufficiently to allow substrate removal. The handle silicon was removed from the SOI substrate by an HF/nitric/acetic acid etch followed by 10% tetramethylammonium hydroxide at 90°C, which is selective to the BOX.

Following substrate removal large openings were etched above the existing source, drain, and gate metal pads. No additional metal deposition was required for this experiment. Because our wafer-wafer bond can tolerate high temperatures, a final sintering was done at 400°C to remove any plasma damage that occurred during contact etch. This differed from our earlier experiment where an epoxy-based bond prevented any subsequent temperature steps in excess of 200°C and resulted in ±50-mV FET threshold voltage variation between pre- and post-bonding.

Additional work is still required to address manufacturing and reliability issues of this fabrication approach. We note that oxide bonding of silicon wafers is a well-established technique used for volume manufacturing of SOI wafers. The technique required for bonding finished integrated circuit wafers is different, primarily in that the temperature must be limited to avoid damage to the circuit. However, we believe that much of the knowledge accumulated in SOI wafer manufacturing should be transferable to volume bonding of integrated circuit wafers. The subsequent wafer removal and pad opening steps are simple ones, easily handled by any integrated circuit facility.

We studied the radiation effects in $L = 0.18$ and 0.5 μm FDSOI nFETs after substrate removal, and then patterned the BOX side of the wafer to locally thin the BOX under the transistor using a timed buffered hydrofluoric acid based wet etch. An atomic force microscope was used to characterize the amount of etched BOX by measuring the step between etched and unetched (masked) regions of the BOX. The remaining BOX thickness was shown to be about 56 nm after etch.

Typical total dose radiation response in the offgate bias of $W = 8$ μm, $L = 0.18$ μm FDSOI nFETs after substrate removal and after BOX thinning to ~56 nm are shown in Figures 7-7 and 7-8, respectively. The I-V curves shown in Figures 7-2, 7-7, and 7-8 pre-radiation are very similar, indicating that the new bonding process and thinning process did not compromise the intrinsic FET properties. In agreement with our earlier experiments [7], the radiation-induced front-gate I-V shift is significantly reduced after substrate removal both below and above threshold. This shift is reduced further when the BOX is thinned to ~56 nm.

Figure 7-9 shows that, after substrate removal, ΔV_{TF}, extracted from the curves in Figure 7-8, is reduced by about half from –0.3 V to below –0.15 V at 1 Mrad (SiO_2). After subsequent thinning of the

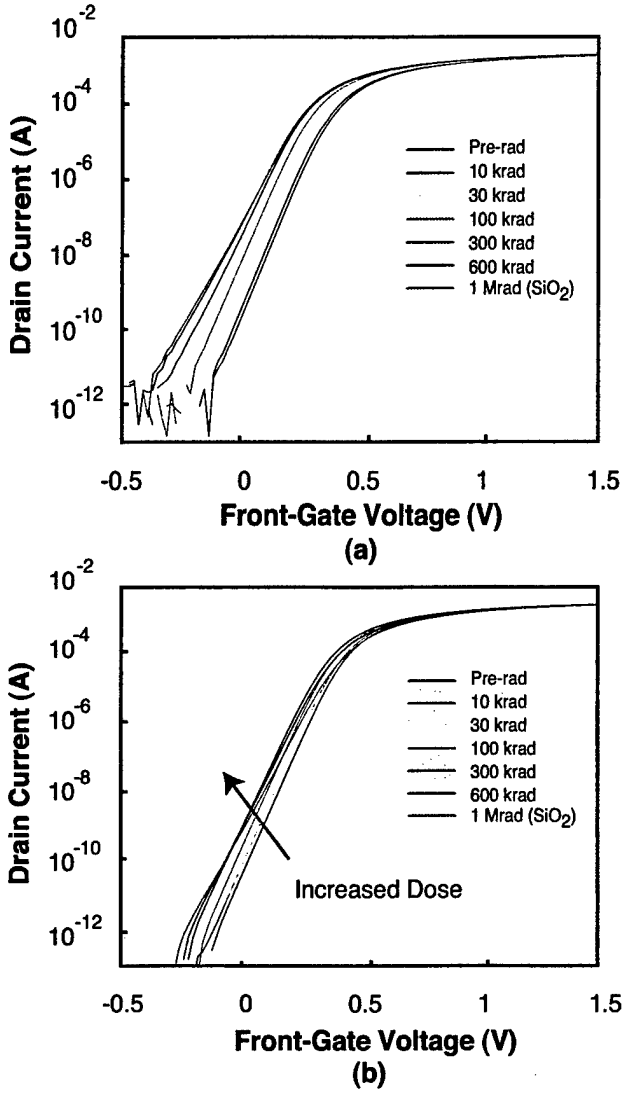

Figure 7-7. Typical front-gate semilogarithmic I-V curves at 50-mV drain bias for W = 8 μm, L = 0.18 μm FDSOI nFET (a) after substrate removal and (b) after BOX thinning.

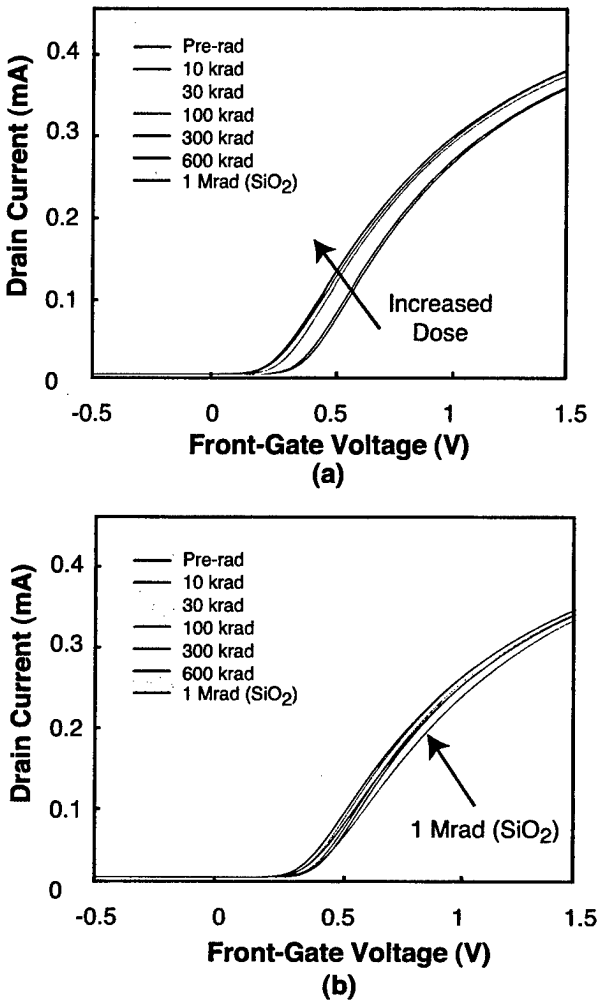

Figure 7-8. Front-gate linear I-V curves at 50-mV drain bias for W = 8 μm, L = 0.18 μm FDSOI nFET (a) after substrate removal and (b) after BOX thinning.

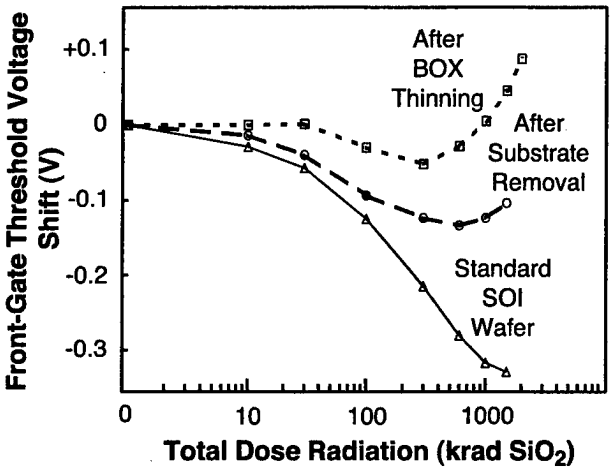

Figure 7-9. Typical ΔV_{TF} vs total dose radiation at 50-mV drain bias for W = 8 μm, L = 0.18 μm FDSOI nFETs on standard wafers, after substrate removal and after BOX thinning.

BOX, ΔV_{TF} was at least four times smaller than for nFETs on standard substrates at the same dose. ΔV_{TF} was also observed to saturate at lower doses after substrate removal and BOX thinning than for nFETs on standard wafers. As shown in Figure 7-9, the saturation dose was around 1,500 krad (SiO_2) for nFETs on standard wafers, 600 krad (SiO_2) after substrate removal, and 300 krad (SiO_2) after BOX thinning for $L = 0.18$ μm nFETs. Above the saturation dose, ΔV_{TF} was observed to turn around, that is, ΔV_{TF} became less negative with total dose. For $L = 0.18$ μm nFETs after BOX thinning, V_{TF} was larger at 1 Mrad (SiO_2) than its pre-radiation value. Consequently, the 1 Mrad I-V curve shown in Figure 7-8(b) has shifted towards positive voltages compared to its pre-radiation position. We noted little degradation in the subthreshold slope and conductance (I-V curves are parallel at high drain current) up to 1 Mrad (SiO_2) after substrate removal and BOX thinning.

Figures 7-10(a) and 7-10(b) show the transconductance G_m vs front-gate voltage at 50 mV on the drain for $L = 0.18$ μm nFETs on standard wafers and after substrate removal. We observed that the maximum transcondutance G_m^{max} remains within 10% of its pre-radiation value even after substrate removal. The front-gate voltage at G_m^{max} decreases with an increase in total dose in the same way as for V_{TF}. Figure 7-10(b) shows that after substrate removal, there is no shoulder associated with a back-channel inversion layer, as exists in Figure 7-10(a) for nFETs on standard wafers. The front-gate G_m vs voltage curves were similar after substrate removal and after BOX thinning, except that after BOX thinning the front-gate voltage at G_m^{max} was larger at 1 Mrad (SiO_2) than pre-radiation. This observation was consistent with the turnaround in ΔV_{TF} shown in Figure 7-9. We also noted that the turnaround was very similar in mesa and H-gate (edgeless) nFETs. Figure 7-11 shows that after substrate removal the radiation-induced ΔV_{TF} was lower for $L = 0.18$ μm than $L = 0.5$ μm nFETs. In contrast, ΔV_{TF} was very similar for the same nFETs on standard substrates.

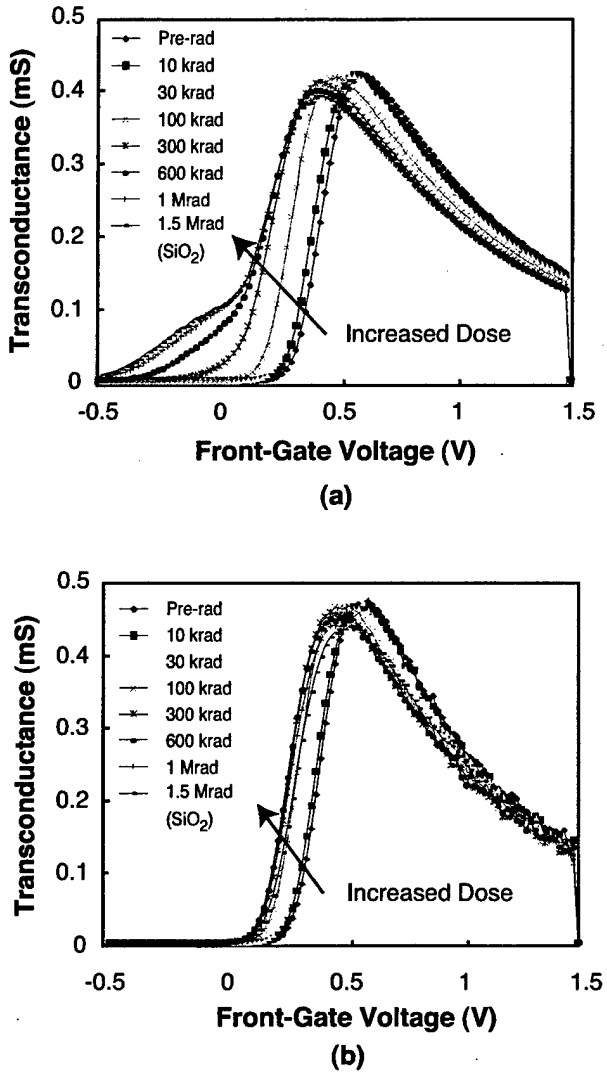

Figure 7-10. Front-gate transconductance $G_m(V)$ curves at 50-mV drain bias for W = 8 μm, L = 0.18 μm FDSOI nFET (a) on standard wafers and (b) after substrate removal.

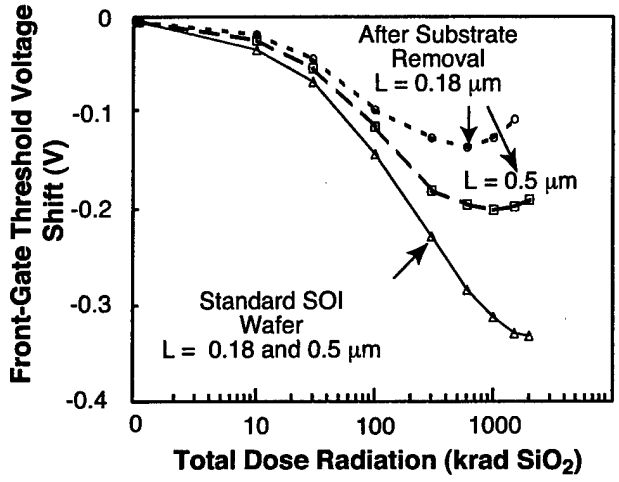

Figure 7-11. Typical ΔV_{TF} vs total dose radiation at 50-mV drain bias for W = 8 μm, L = 0.18 and 0.5 μm FDSOI nFETs on standard wafers and after substrate removal.

Radiation testing was also done for $W = 8$ μm, $L = 0.18$ μm nFETs in the ongate bias condition during irradiation. Figure 7-12 shows that ΔV_{TF} was also reduced after substrate removal under the ongate bias condition. Offgate is still worse than ongate bias after substrate removal and BOX thinning.

After removal of the substrate, the potential of the newly exposed surface of the buried oxide is no longer controlled. We speculated that charge might be present at that surface, in which case it would affect the threshold voltage. Any such charge would be affected by lateral surface conduction, and one would expect the surface conductivity to increase with increasing ambient humidity. To look for any such effect, we irradiated transistors with a dry or wet ambient above the BOX.

The dry ambient was achieved by delivering pure N_2 gas through a small nozzle mounted above the wafer near the BOX-side of the nFET under test. The wet ambient was achieved by running the N_2 through a bubbler full of water. The humidity level was evaluated before radiation testing with a humidity sensor placed on the wafer chuck. We measured humidity levels greater than 55% for the wet condition, and below 20% for the dry one. In both cases, the wet or dry N_2 gas was allowed to flow above the device for 20 min prior to turning on the x-ray source. As shown in Figure 7-13, we did not observe a significant difference between room, wet, and dry ambient conditions after substrate removal. This result suggests that surface charging at the BOX/air interface does not play a major role in the total dose response of nFETs after substrate removal.

After these experiments were completed, we used 2D Atlas to simulate the potential contour lines in the BOX for an $L = 0.18$ μm nFET on a standard wafer and after substrate removal in the offgate bias. In the simulations, we assumed that the air was an insulator with a relative permittivity equal to 1.

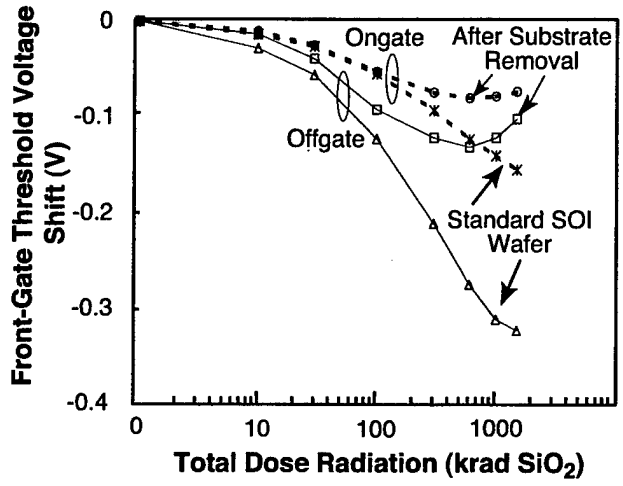

Figure 7-12. Typical ΔV_{TF} vs total dose radiation at 50-mV drain bias for W = 8 μm, L = 0.18 μm FDSOI nFETs on standard wafers and after substrate removal in the ongate and offgate bias condition during irradiation.

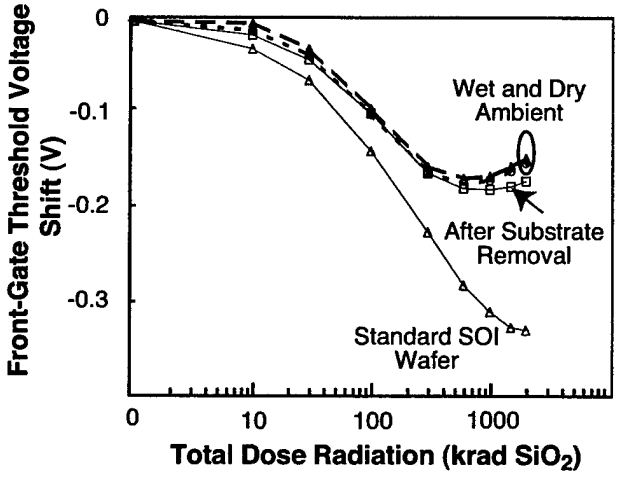

Figure 7-13. Typical ΔV_{TF} vs total dose radiation at 50-mV drain bias for W = 8 μm, L = 0.5 μm FDSOI nFETs on standard wafers after substrate removal (room temperature testing) and after substrate removal with a wet and dry ambient above the BOX/air interface.

As shown in Figure 7-14(a), on the standard wafer the electric field in the BOX, which is perpendicular to the potential contour lines, points toward the BOX/substrate interface under the drain, and toward the transistor body. As proposed by other authors [11], it is the hole trapping under the body that causes ΔQ_{NET} to be positive. Holes trapped under the drain at the BOX/substrate interface have little effect on the potential at the SOI/BOX interface. ΔQ_{NET} increases with total dose because the number of radiation-induced trapped holes increases with dose. The radiation-induced ΔV_{TF} saturates experimentally around 1 Mrad (SiO_2) because the maximum hole trap density is reached. Electron trapping does not play a major role at doses below 2 Mrad (SiO_2).

As shown in Figure 7-14(b), after substrate removal the electric field in the BOX is mostly directed toward the transistor body. Therefore, hole trapping under the body should be even larger after substrate removal than for nFETs on standard substrates, which is not in agreement with our experimental results. The electron-hole interaction yielding to charge trapping could be different after substrate removal and BOX thinning, but we cannot specifically say what has changed solely based on our results. We can only postulate that electrons play a dominant role in the charge-trapping process after substrate removal and BOX thinning. Indeed, the turnaround in ΔV_{TF} for $L = 0.18$ μm nFETs after BOX thinning indicates that positively charged traps are compensated by negatively charged traps. When V_{TF} becomes larger than its pre-radiation value, then ΔQ_{NET} imaged under the body has become negative, which means that electron traps (fixed charges in BOX or interface traps) contribute to the nFET radiation response at doses below 2 Mrad (SiO_2) after substrate removal and BOX thinning.

We have considered the possibility that removal of the substrate may allow the stress in the (formerly) buried oxide to relax, possibly changing its trapping properties. Passivation layers deposited on top of the buried oxide for long-term reliability may also affect the charge trapping. These are important areas of future research.

In conclusion, we present new total dose radiation test results for an $L = 0.18$ μm FDSOI mesa nFET on conventional Unibond wafers with 200-nm BOX. We analyze experimental results with a one-dimensional model and demonstrate that total dose radiation effects were entirely due to radiation-induced positive charges in the BOX with no strong edge effects in offgate bias condition.

We also present new results on FDSOI FETs after substrate removal and BOX thinning. We show that the radiation-induced shift in the front-gate I-V is significantly reduced above and below threshold at 50-mV drain bias compared to FDSOI FETs on conventional SOI wafers in both ongate and offgate bias, for $L = 0.18$ and 0.5 μm. The reduction was always enhanced after BOX thinning. We also show that a dry or wet ambient above the BOX/air interface has little effect on the radiation response after substrate removal. Our experimental results indicate that electrons are playing an important role in the radiation-induced trapping process after substrate removal and BOX thinning.

Substrate removal and BOX thinning may provide a new option for fabricating submicron integrated circuits with enhanced tolerance to ionizing radiation. Manufacturability and reliability issues of the process, including effects of a passivation insulator on the outer surface of the BOX, have yet to be explored. We note that the additional processing required is fully compatible with standard FDSOI CMOS

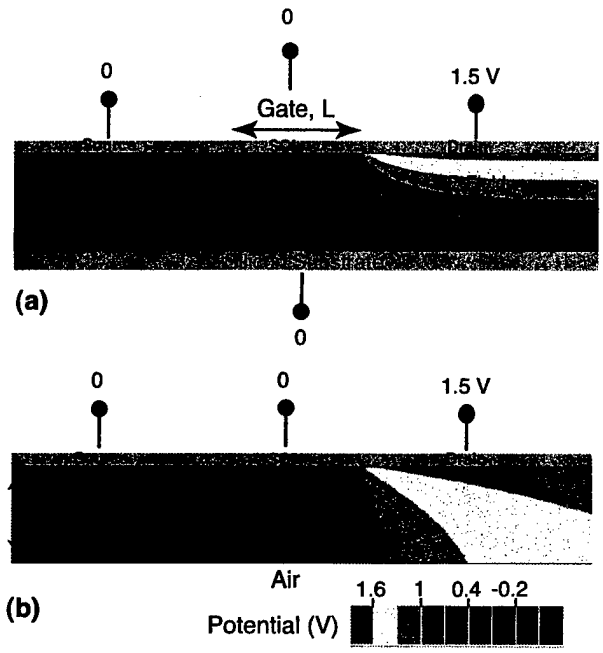

Figure 7-14. Potential contour lines with 1.5-V drain bias (as in offgate bias condition) for L = 0.18 μm FDSOI nFET (a) on standard wafers and (b) after substrate removal (potential in Atlas is voltage minus Fermi potential).

wafer processing. This technology is also of interest for rf applications since the parasitic coupling to the substrate is suppressed [12]. This technology might also provide more tolerance to single-event upsets since charge collection at the BOX/substrate is no longer possible [13].

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This report covers in detail the research work of the Solid State Division at Lincoln Laboratory for the period 1 May–31 July 2003. The topics covered are Quantum Electronics, Electro-optical Materials and Devices, Submicrometer Technology, Biosensor and Molecular Technologies, Advanced Imaging Technology, Analog Device Technology, and Advanced Silicon Technology. Funding is provided by several DoD organizations—including the Air Force, Army, DARPA, MDA, Navy, NSA, and OSD—and also by the DOE, NASA, and NIST.

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materials research	advanced imaging technology	flip-chip devices	quantum computing
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